DESIGN AND FABRICATION OF A HYPERABRUPT VARIABLE CAPACITANCE DIODE

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By
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CERTIFICATE

This is to certify that the thesis entitled 'Design and Fabrication of a Hyperabrupt Variable Capacitance Diode' by P.N. Goswami is a record of work carried out under my supervision and has not been submitted elsewhere for a degree.

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ABSTRACT

Design of a hyperabrupt varicap needs knowledge of breakdown voltage 'V_B', the capacitance ratio 'R_c' and the cutoff frequency 'f_{c3}' as a function of different profile parameters. In the present work, the capacitance ratio and the cutoff frequency have been calculated as a function of surface concentration 'N_s', background to surface concentration ratio 'R_c' and the characteristic length 'Z'. In these calculations, a one sided hyperabrupt junction with exponentially doped retrograded region has been assumed. The built_in voltage needed for the determination of the capacitance ratio is also calculated. The cutoff frequency of the diode has been calculated assuming the epilayer thickness of the wafer to be just equal to the depletion region width at the maximum operating voltage of the device. A hyperabrupt varicap diode has been designed using the plots based on the above information. Silicon hyperabrupt diodes are fabricated on the basis of above design by double diffusion technique. The retrograded region of the device is formed using commercially available phosphorosilica film. The doping profile of the device has been investigated using C-V technique. Though, the required surface concentration could not be achieved in the particular run, but the results of measurements were in agreement with those obtained from the plots derived above.

The various limitations of the fabricated device have been discussed and suggestions made for further improvement. Lastly, a new method of fabricating a hyperabrupt varicap with low values of 'Z' and high value of 'R_c' ($>$ 0.1), has been suggested using phosphorus rejecting property of a growing oxide on the silicon surface.

NOMENCLATURE

q	Electronic charge
ϵ	Permittivity of silicon
k	Boltzmann constant
n	C-V index
x	Distance from the junction
R_c	Ratio of 'N_B' to 'N_o'.
A	Junction area
C	Capacitance of the junction
$C_j(V)$	Junction capacitance at a reverse bias of V volts
C_3	Junction capacitance at a reverse bias of 3 volts
C_{25}	Junction capacitance at a reverse bias of 25volts
C_3/C_{25}	Ratio of the junction capacitances at reverse bias of 3 volts and 25 volts
$(C_3/C_{25})_{max}$	Maximum value of 'C_3/C_{25}'
E	Electric field at 'x'
fc_V	Cutoff frequency of the junction at a reverse bias of V volts
$N_D(x)$or $N(x)$	Donor concentration at 'x'
$N_A(x)$	Acceptor concentration at 'x'
N_o	Cross over impurity concentration in the retrograded region
N_B	Background impurity concentration
$R_s(V)$	Series resistance of the junction at a reverse bias of V volts

V	Potential at 'x'
V_B	Breakdown voltage
V_o	Built-in voltage of the junction
V_a	Voltage applied across the device
$V(W)$	Voltage drop across the depletion region
W	Depletion region width
W_3	Depletion layer width at a reverse bias of 3 volts
W_{25}	Depletion layer width at a reverse bias of 25 volts
Z	Characteristic length
Z_{opt}	Value of Z at which $(C_3/C_{25})_{max}$ occurs for a given 'N_o'
σ_{av}	average conductivity
$\sigma(x)$	conductivity at 'x'
$\mu(x)$	mobility at 'x'

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CHAPTER I

INTRODUCTION

The VARIable CAPacitance diode (commonly known as Varactor in the microwave frequency range) is primarily a p-n junction diode which is used for its voltage dependent reactive properties in reverse bias.

Varactors find their use mainly in the high frequency range which extends from VHF to millimeter wave region. These ar used for voltage controlled frequency tuning, harmonic generation parametric amplification, switching of microwave signals, continu phase shifting, frequency modulation etc.

The basic element of a varactor is its junction capacitanc It is, therefore, desirable that all other parasitic effects like series resistance, shunt resistance and fixed reactances be minimi The junction capacitance at a given reverse bias depends upon the depletion layer width at that voltage. Therefore, by controlling the doping profile across the junction, a varactor can be tailored to suit a particular application.

When the doping concentration near the junction changes abruptly (i.e., the change takes place over a few lattice spacings the diode is recognised as an abrupt junction diode. Conversely, if the doping profile is graded all throughout the entire excursio of the depletion layer, from zero bias to breakdown, then it is known as a graded junction diode. Linearly graded junction diode is one amongst the class of graded junction diodes. Abrupt juncti

varactors are normally fabricated by alloying process or by making a Schottky-barrier contact, while graded junction varactors are made by deep diffusion or by epitaxial growth.

Both the abrupt junction and the linearly graded junction can be characterised by an exponent 'n' which is known as C-V index*. This exponent 'n' defines a linear relationship between the junction capacitance 'C' and the applied reverse volta 'V' of the form $C \propto V^{-n}$. For an abrupt junction, value of 'n' is one-half and for a linearly graded junction, its value is one-third. For intermediate forms between these two extremes, where the grading in the transition region varies from a very slight exponential to a steep exponential, C-V index can range from one-third to one-half, and may not remain constant over the total voltage excursion range. These forms are often recognised as hybrid junctions.

Hyper-abrupt junctions belong to the class of hybrid junctions. Hyper-abrupt varactors are peculiar due to their high C-V index, which is always more than one-half (Typical values are 4 to 5). This type of varactor could be produced by forming an abrupt junction between two substrates of opposite type in which the doping concentrations decrease with distance from the junction. The region having the decreasing concentration is known as retro-graded region. The junction could be a one-sided junction as well.

*Alternatively, C-V index can be defined as $n=d(\log C)/d(\log V)$.

One sided hyper-abrupt varactors can be made by forming a junction between a heavily doped substrate of one type and another substrate with retrograded region of other type. Owing to the ease of fabrication of one-sided junctions using conventional techniques, these junctions are always preferred over both-sided junctions. The retrograded region can be formed by diffusion, epitaxial growth or by ion implantation techniques [16,17]. Depending upon the fabrication process, the retrograded region can assume any of the following distributions, viz., erfc, gaussian, exponential power-law or a mixture of these. The abrupt junction, on top of the retrograded region, is formed by alloying, shallow diffusion or by making Schottky contacts.

With increasing reverse bias, the movement of depletion layer in hyper-abrupt diodes is continuously into a region of lighter and lighter doping. As a result, the junction capacitance of these diodes decrease much faster as compared to abrupt and graded junction diodes. The microwave varactors usually employ linearly graded junctions. Hyper-abrupt varactors find limited use in this frequency range because of their lower cut-off frequency. This is due to the fact that the decreasing doping concentration of the retrograded region in a hyper-abrupt varactor offers a higher series resistance at lower reverse voltages.

To minimise the varactor series resistance, the

retrograded base region is made thin enough so that the depletion layer at breakdown extends completely through this region and touches the ohmic contact. Since the normal width requirement of the base region is of the order of a few microns, hyperabrupt varactors are invariably fabricated on heavily doped epitaxial substrate with the required thin base region on top of it.

The present work was started with a view to design and develop a hyperabrupt varactor for voltage tuning in the VHF range (30 to 300 MHz). These diodes find immediate use in TV tuners and FM receivers. The operating voltage range of these devices is normally from 3 to 25 volts. The important design parameters of a varactor are: the junction capacitance and its voltage sensitivity the series resistance associated with the semiconductor material and the breakdown voltage. All these parameters are determined by the impurity distribution in the retrograded region.

To relate the device parameters to the details of the impurity profile, we need a computer programme which can give the optimum values of profile constants for the required device characteristics. A general approach may be to consider all the practical profiles for the retrograded region and choose the one which predicts the best performance. Gaussian profile has been discussed in detail by Kannam et al [1]. Power-law distribution has also been investigated [2] and fabricated recently using computer controlled epitaxial growth reactor [3]. Shinoda [4]

has calculated the C-V characteristics of Erfc profiles. Simiju [5] has discussed the C-V characteristics of the exponential distribution and Clk [6] has discussed the same profile as an approximatio to the profiles obtained by diffusion and has analysed it in detail.

Exponential distribution assumes importance due to its simplicity of analysis and also because it is a good approximation to the impurity profiles obtained by diffusion . Information regarding the breakdown voltage of exponentially retrograded p^+-n junctions is available in the literature [7] . None seems to have discussed the dependence of capacitance ratio ($C3/C_{25}$) on different profile parameters, viz., crossover concentration 'N_o', background to surface concentration ratio 'R_c' and profile constant 'Z'. Also little information is available regarding the dependence of cut-off frequency on these different profile parameters. In the present work exponentially doped retrograded region has been chosen for the reasons given above. The following specific studies were planned

(a) To calculate the built-in voltage 'V_o' of one-sided junction for different values of N_o, R_c and Z and to calculate the capacitance ratio C_3/C_{25} using this information.

(b) To determine the cut-off frequency fc_3 (at a reverse bias of 3 volts), corresponding to all the sets of values of N_o, R_c and Z discussed above.

(c) To characterize some of the commonly available varicaps

presently used for tuning in the VHF range. This was done with a view to obtain information about the impurity profile of the device.

(d) To fabricate units for carrying out measurements to verify the results of the theoretical calculations.

CHAPTER II

CAPACITANCE RATIO 'C_3/C_{25}' AND CUT'OFF FREQUENCY 'fc_3'

2.1 Theoretical Considerations

For the analysis carried out in this chapter, the following assumptions have been made:

(1) The junction considered is one sided p^+-n in which the transition is abrupt and the p-side is so heavily doped that the fermilevel on this side coincides with the upper edge of the valence band.

(2) The impurity distribution in the retrograded n-side decreases exponentially with the distance from the junction.

This assumed distribution is shown in Fig.(1).

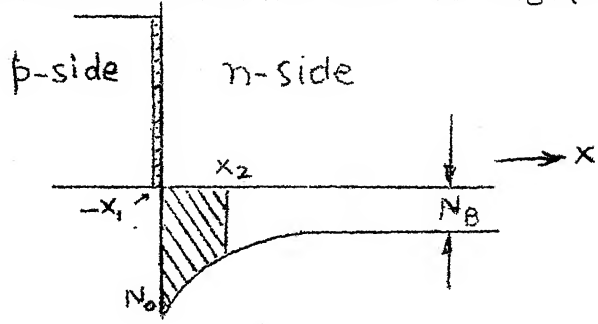

Fig.(1)

The impurity distribution in the retrograded region can be represented as

$$N_D(x) = (N_o - N_B)\, e^{-x/z} + N_B \qquad (1)$$

where 'N_o' is the concentration of the retrograded region at the junction (i.e., at x=0), 'N_B', the background concentration,

'z', the characteristic length and 'x', the distance measured from the junction.

Under reverse bias, the junction space charge region extends mainly in the retrograded side, since the other side is heavily doped. Potential distribution in this region can be determined from the solution of one-dimensional Poisson's equation

$$\frac{d^2V}{dx^2} = -\frac{q}{\epsilon} \cdot N_D(x) \qquad (2)$$

In writing this relation it has been assumed that all the impurity atoms are ionised and the mobile carrier concentration in the space charge layer is negligible.

Integrating equation (2), twice with respect to x, with the following boundary conditions

$$E = 0 \text{ at } x = W$$
$$\text{and } V = 0 \text{ at } x = 0 \qquad (3)$$

leads to

$$V(W) = V_a + V_o = \frac{q}{\epsilon} N_o z^2 \left\{ (1-R_c)(1-(1+W/z)e^{-W/z}) - \frac{R_c}{2} \cdot \left(\frac{W}{z}\right)^2 \right\} \qquad (4)$$

where V_a = Applied voltage across the junction

V_o = Built-in voltage of the junction

$R_c = N_B/N_o$

E = electric field at distance 'x'

and W = depletion layer edge on the retrograded side.

The depletion region capacitance 'C' can be written as

$$C = \frac{\epsilon}{W} \cdot A \qquad (5)$$

where 'A' represents the junction area.

Equation (4) is an analytical expression between V&W (hence, also between V&C) in transcedental form. Normally we need an expression of the form C =f(V) (capacitance, a function of voltage) instead of V = g(C) (voltage, a function of capacitance). Solving equation (4) explicitly for 'W' is not possible, therefore, it is not an easy matter to study the effect of parameters N_o, R_c and z on the C-V characteristics. However, we can solve equation (4) on computer iteratively to study the effect of these parameters.

Our main interest in the study of C-V characteristics is to find capacitance ratio' C_3/C_{25}' which is defined as the ratio of junction capacitances at V_a=3V and V_a = 25V. The other unknown appearing in these calculations is the built-in voltage of the junction . Since, no information is available in the literature regarding built-in voltage of junctions with exponentially doped retrograded region, it has to be calculated first.

2.2 Calculation of Built-in Voltage 'V_o'

The built-in voltage 'V_o' of a junction can be calculated if the doping concentrations at the edges of the depletions region under thermal equilibrium are known, using the relation

$$V_o = \frac{kT}{q} \cdot \ln \frac{N_A(-x_1) \cdot N_D(x_2)}{n_i^2} \qquad (6)$$

Where '$N_A(-x_1)$' is the acceptor concentration at the depletion region edge on p-side, '$N_D(x_2)$', the donor concentration

at the depletion region edge on n-side and 'n_i', the intrinsic carrier concentration at 300°K.

Assuming a heavily doped p-side and neglecting the related band-gap narrowing effects, relation (6) can be rewritten as

$$V_o = .55 + \frac{kT}{q} \ln \frac{N_D(x_2)}{n_i} \qquad (7)$$

$N_D(x)$ continuously varies in the retrograded region, therefore, without the knowledge of exact location of 'x_2', we cannot find 'V_o' from equation (7).

Second relation for V_o is obtained by substituting $V_a = 0$ in equation (4), rewritten as follows

$$V_o = \frac{q}{\epsilon} N_o Z^2 \left[(1-R_c)\left\{1-(1+\frac{x_2}{Z})\, e^{-x_2/Z}\right\} - \frac{R_c}{2}\left(\frac{x_2}{Z}\right)^2 \right] \qquad (8)$$

Equation (7) determines the built-in voltage by finding the difference between the fermi level on the two edges of the depletion region and equation (8) determines the same by integrating twice over the charge enclosed within the depletion region. Individually, both the equations (7) and (8) are incapable of giving the value of V_o, but their simultaneous solution can determine a unique value of it. 'x_2' is assigned an arbitrary value and V_o is calculated using expressions (7) and (8). Depending on the difference between the two values of V_o, thus calculated, value assigned to 'x_2' is modified and calculations continued till the difference comes within .1%. This value of V_o is the built-in

voltage of the junction and the value of 'x_2' assigned last is the zero bias depletion layer width of the junction.

The calculated values of V_o are plotted as a function of N_o for different values of R_c & Z, in figs.(2) to (5).

It is seen that, for values of 'Z' in excess of 1.0μ, the built-in voltage increases more or less linearly with log N_o, for all the values of N_o and R_c. The same is also true for values of N_o exceeding $2x10^{17}/cm^3$ for all the values of R_c and Z. In these regions, the junction behaves like an abrupt junction because the zero bias depletion region width is small enough to approximate the value of $N_D(x_2)$ as N_o itself.

Similarly, for smaller values of Z (lower than .3μ) and low values of N_o, the zero bias depletion region extends beyond the retrograded region and $N_D(x_2)$ can be approximated by N_B. In this region also, the junction behaviour is similar to that of an abrupt junction. For intermediate values of N_o and values of Z, less than 1.0μ, $N_D(x_2)$ lies within N_o and N_B. In this region, hyperabrupt nature of the junction is predominantly shown.

2.3 Capacitance Ratio 'C_3/C_{25}'

To calculate junction capacitance at a given reverse bias we need to know the depletion region width 'W' at that voltage. Since we do not have an explicit expression which can directly find the depletion layer width for a given voltage, we need to use

expression (4) iteratively to relate the two. Depletion region width W is assigned an arbitrary value in expression (4) and V(W) calculated. Depending upon the difference between the calculated value of V(W) and actual value (V_o+V_a), W is modified and V(W) recalculated, till the difference between the two falls within .1%. Depletion layer widths were calculated for reverse bias of 3 volts and 25 volts. The inverse ratio of these two widths directly give the capacitance ratio.

Capacitance ratio 'C_3/C_{25}' has been calculated for a number of values of R_c (.01, .02, .05 & .1) and 'Z' (.1, .3, .536, 1.06, 1.93, 2.94, 4.76 μ) at different values of N_o (in the range $2\times10^{15}/cm^3$ to $5\times10^{17}/cm^3$). It is seen that $(C_3/C_{25})_{max}$ (maximum value of C_3/C_{25}) occurs at the same value of N_o, at a given Z, for different values of R_c. Also, value of $(C_3/C_{25})_{max}$ is independent of 'Z' for a given R_c. For values of N_o an order of magnitude higher and lower than $(N_o)_{max}$ (defined as the value of N_o at which capacitance ratio is maximum for a given 'Z'), the ratio 'C_3/C_{25}' approaches $\sqrt{\frac{V_2+V_o}{V_1+V_o}}$, which is a characteristic of an abrupt junction. The dotted portion of the curve is unachievable as the breakdown in this region is less than 25 volts.

Theoretical justification that $(C_3/C_{25})_{max}$ occurs at the same value of N_o for different values of 'R_c', is given in the

following steps.

At the value of maximum 'C_3/C_{25}', condition

$$\frac{d(C_3/C_{25})}{dN_o} = 0 \qquad (9)$$

must be satisfied.

Equation (9) lead to the condition

$$C_3 \propto \frac{dc_3}{dN_o} \quad \text{or} \quad C_{25} \propto \frac{dc_{25}}{dN_o}$$

using equation (5), we get a general condition

$$W \propto \frac{dw}{dN_o} \quad \text{or} \quad W = M \frac{dw}{dN_o} \qquad (10)$$

here, 'M' is a proportionately constant having dimensions of Cm^{-3}.

For values of $R_c < .1$, $(1-R_c)$ term in equation (4) can be dropped

Differentiating the modified equation (4) with respect to N_o and substituting maxima condition of equation (10), we get

$$\frac{1}{(N_o)^2_{max}} = \frac{q}{\epsilon} \frac{Z^2}{V(W)} \cdot \frac{1}{M} \left[-\left(\frac{W}{Z}\right)^2 \cdot e^{-W/Z} + R_c \left(\frac{W}{Z}\right)^2 \right] \qquad (10)a$$

Equation (4) can be used to eliminate R_c from (10)a.

$$\frac{1}{(N_o)^2_{max}} = \frac{q}{\epsilon} \frac{Z^2}{V(W)} \cdot \frac{1}{M} \left[1 - \left\{ \frac{1}{2} \cdot \left(\frac{W}{Z}\right)^2 + \left(\frac{W}{Z}\right) + 1 \right\} e^{-W/Z} \right] - \frac{1}{(N_o)_{max} \cdot M} \qquad (11)$$

This expression is independent of R_c, which implies that $(N_o)_{max}$ is the same for all values of $R_c < .1$.

Figure (10) shows a plot between Z_{opt} (defined as the value of 'Z' at which maximum of (C_3/C_{25}) occurs for a given value of N_o) and N_o. For the presently considered range of values of 'N_o' and 'Z', it is seen that log Z_{opt} varies linearly with log N_o.

Fig(10)a is a similar plot between $(C_3/C_{25})_{max}$ and R_c. The information for these plots has been derived from Figs.(6) to (9). Figs(10) & (10)a are useful for the design of a varicap (see Chap.III)

2.4 Cutoff Frequency 'f_{C_3}' and Minimum epilayer Thickness 'W_M'

At a given operating voltage, the diode series resistance 'R_s' and the junction capacitance 'C_j' determine the cut-off frequency of a varactor

$$f_{C_V} = 1/2\pi \quad R_s(V).\ C_j(V) \qquad (12)$$

To maximise the cut-off frequency of a varactor we need to choose the highest dopant concentration compatible with the desired breakdown voltage.

The minimum epilayer thickness 'W_M' required for a device structure is the width of depletion region at maximum operating voltage, i.e., 25 volts. In figs (11) to (14), this minimum thickness has been plotted as a function of N_o for various values of R_c and Z. The dotted portion of the curves correspond to the epilayer thickness which have a breakdown voltage of less than 25 volts. For values of 'Z' less than .5 μ, minimum epilayer thickness W_M decreases linearly with increasing log N_o in the range $2\times10^{15}/cm^3$ to $3\times10^{16}/cm^3$ for all the values of 'R_c'. Similarly, for values of 'Z' more than 1.0 μ, W_M decreases linearly with increasing log N_o in the range $3\times10^{16}/cm^3$ to $5\times10^{17}/cm^3$ for all the values of R_c. All the curves for different values of 'Z' are bounded between two straight lines

which correspond to minimum epilayer thicknesses for abrupt junctions with doping N_o and N_B.

Cut off frequency 'fc_3' has been calculated at a reverse bias of 3 volts using relation of equation (12). The corresponding junction capacitance '$C_j(3)$' has been calculated using equations (4) and (5). The diode series resistance $R_s(3)$ has been evaluated using the following relations:

$$R_s(3) = \frac{W_{25}-W_3}{\sigma_{av}.\ A} \tag{13}$$

$$\sigma_{av} = \frac{1}{W_{25}-W_3} \int_{W_3}^{W_{25}} \sigma\,(x)dx \tag{14}$$

$$\sigma(x) = q.\ N_D(x).\ \mu(x) \tag{15}$$

$$\mu(x) = \frac{\mu_{max} - \mu_{min}}{1 + \left(\frac{N_D(x)}{N_{REF}}\right)^{\alpha}} + \mu_{min} \tag{16}$$

where 'σ_{av}' is the average conductivity of undepleted layer, $\sigma(x)$, the conductivity at any distance 'x', $\mu(x)$, the electron mobility at 'x' and 'μ_{max}', 'μ_{min}', 'α' and 'N_{REF}' are constants having values μ_{max} = 1330 $cm^2/sec.$, μ_{min}=65 $cm^2/sec.$ α= .72 and $N_{REF}=8.5\times10^{16}/cm^3$ [1]. The integral in equation (14) was evaluated using Simpson's rule. For calculating the cut-off frequency, it has been assumed that the resistance contributions from substrate and the ohmic contacts are negligible compared to the active semiconductor resistance.

Plots of cut off frequency 'fc_3' as a function of N_o for the already considered values of R_c and Z are shown in figures (15) to (18). From the plots of figures (17) and (18), it is seen that the cut off frequency increases monotonically with increasing values of N_o. This is understandable because with increasing N_o, decrease in $R_j(3)$ is more pronounced as compared to the increase in $C_j(3)$. The sharp decrease in $R_j(3)$ is contributed by decreasing epilayer thickness besides increase in the conductivity of the background region with increasing N_o.

A dip in the fc_3 v/s N_o curves of figs. (15) and (16), corresponding to low values of R_c, can be observed. This dip corresponds to the value of N_o for which the depletion region width 'W_3' is situated on the sharp gradient in the retrograded region and the width 'W_{25}' is extending in the low gradient region, where the concentration approaches N_B. Under this condition, an increase in N_a causes a sharp increase in the junction capacitance '$C_j(3)$' but the reduction in series resistance is normal. This causes a decrease in the cut off frequency till 'W_{25}' also lies on the sharp gradient of the retrograded region.

For large values of Z at high N_o, all the curves merge with the cut off frequency curve of an abrupt junction with n-side doping equal to N_o, while for lower values of 'Z' at low N_a, the curves merge with the cut off frequency curve of an abrupt junction with n-side doping equal to N_B.

CHAPTER III

CHARACTERIZATION OF AVAILABLE VARICAP DIODE

3.1 Specifications of the Device

To get an idea of circuit requirements of the varicaps used in the VHF range, specifications of some of the commonly used devices were studied and one of them was characterised for obtaining information about the impurity profile of the device. The device selected for characterization was a varicap BB 106 of Philips make (extensively used in TV tuners). The device is a silicon planar variable capacitance diode with the following specifications provided by the manufacturer (Table 3.1).

Maximum Forward current I_F	= 20 mA
Cont. peak reverse voltage V_R	= 28 volts
Repititive peak reverse voltage V_{RRM}	= 30 volts
Junction temperature T_j	= 60°C
Storage temperature T_{stg}	= 100°C
Thermal resistance (Jn. to amb.) $R_{th_{j-a}}$	= 400°C/watt
Leakage current at -28V(25°C)	< .05 μA
Leakage current at -28V(60°C)	< 0.2 μA
Junction capacitance at (V_R=3V)	> 20 pf
Junction capacitance at (V_R=25V) (frequency of measurement = 0.5 MHz)	= 4.0 to 5.6 pf
Diode series resistance 'r_D' at (C_D=25pf)	= 0.4 ohm
Capacitance ratio 'C_3/C_{25}' (on the average)	= 5

Table 3.1

For comparison, specifications of some of the equivalent varicaps manufactured by NEC (Japan) were also checked and it was found that the capacitance ratio varied from 4 to 6, while 'r_D' could be as high as 1 ohm. The junction capacitance at 25 volts varied from 10 pf to 30 pf depending upon the particular application of the device.

3.2. Measurement of C-V characteristics for estimating the Impurity Profile:

The junction capacitance as a function of voltage was measured on one of the units of BB106, both in forward and reverse directions. The measurements in the reverse direction were taken upto the breakdown voltage of the device and in forward direction upto the voltage after which the shunt conductance of the device starts affecting the capacitance measurements. Built-in voltage of the device was estimated by determining the intercept of the $1/C^2$ v/s V_a plot on the voltage axis. A plot of junction capacitance as a function of applied voltage is shown in Fig.(19). Fig.(20) shows the corresponding $1/C^2$ v/s V_a plot of the device. The lower portion of the plot has been drawn on a different scale for clarity. The impurity distribution in the retrograded region has been estimated by measuring the slope $d(1/c^2)/dV$ at a number of points. At any voltag $V(W)$; $N(W)$ and the corresponding 'W' can be calculated using the following equations

$$A^2, N(W) = \frac{2}{qe} \cdot \frac{1}{d(1/C^2)/dV} \qquad (17)$$

$$\frac{W}{A} = \frac{\epsilon}{C} \qquad (18)$$

Since area of the device is not known, we can only relate $A^2.N(W)$ to W/A. Figure (21) shows $A^2.N(W)$ plotted as a function of W/A for the device. From this plot, it is seen that the diode is fabricated on an epitaxial substrate. The profile appears to be a gaussian with surface conc.N_s but in the region from 3 volts to 25 volts, it can be approximated by an exponential distribution to a fair degree of accuracy. The extraploted curve for the equivalent exponential distribution has been drawn on the same graph. The epilayer thickness is just sufficient to sustain the space charge layer at 25 volts. Some calculated results for N_s, N_o, N_B, W_M and Z for different assumed areas of the device are given in Table 3.2. R_c for the varicap, as observed from the graph of Fig.(21), has a value of .04.

Dia of circular dot (in mm)	Area A (in cm^2)	N_s ($in^s cm^{-3}$)	N_o ($in^o cm^{-3}$)	N_B ($in^B Cm^{-3}$)	W_M (in μ)	Z (in μ)
0.2	3.14×10^{-4}	3.0×10^{17}	5.0×10^{17}	2.0×10^{16}	.74	.047
0.3	7.85×10^{-4}	6.0×10^{16}	1.0×10^{17}	4.0×10^{15}	1.67	.11
0.4	12.56×10^{-4}	1.86×10^{16}	3.1×10^{16}	1.25×10^{15}	2.96	.19
0.5	19.6×10^{-4}	7.8×10^{15}	1.3×10^{16}	5.0×10^{14}	4.63	.294
0.6	28.3×10^{-4}	3.7×10^{15}	6.2×10^{15}	2.5×10^{14}	6.67	.423
0.8	50.0×10^{-4}	1.2×10^{15}	2.0×10^{15}	7.8×10^{13}	11.8	.75

Table 3.2

Although, all the combinations of Table 3.2 display the same C-V characteristics, the parameter V_B and R_s have different values for each of the tabulated combinations. The measured device had a breakdown voltage of 40 volts. Assuming the low doped side of the device to be uniformly doped, with a donor concentration N_s, breakdown v/s concentration graphs of [21] give a value of N_s as $5.0 \times 10^{16}/cm^3$. The corresponding calculated value of N_o is $8.33 \times 10^{16}/cm^3$. The expected device area, therefore, comes to 8.0×10^{-4} cm^2 (a dot diameter of 0.3 mm).

CHAPTER IV

DEVICE FABRICATION AND MEASUREMENTS

4.1 Design Considerations

Given a capacitance ratio 'C_3/C_{25}', minimum breakdown voltage 'V_B', junction capacitance 'C_3' or 'C_{25}' and maximum series resistance 'R_s', we can find a suitable combination of N_o, R_c, Z and A which will give the desired values of all the above parameters. As evident from table 3.2, there are many combinations of N_o, R_c, Z and A which meet all these requirements. We, therefore, further need to squeeze the design in view of technological limitations and other inherent distortions in the device characteristics associated with smaller values of R_c. Particularly, devices with value of R_c less than 6.0×10^{-3}, are always associated with an inflexion point in their C-V characteristics [6]. Also, smaller values of R_c lead to lower cut off frequency and higher spread in the device characteristics. These considerations suggest a choice of the highest possible value of R_c to achieve a given capcitance ratio.

Based on the information of chapter III, it was decided to design a varicap with a minimum capacitance ratio of 5, junction capacitance at 25 volts of 5.0 pf and minimum breakdown voltage of 30 volts capable of operating in the VHF range (30-300 MHz). Taking into account the possible spread, the design was aimed to achieve a capacitance ratio of 6, breakdown voltage of 40 volts and the junction capacitance C_{25} of 5.0 pf. From the plots of

Fig.10(a), it is seen that to achieve this capacitance ratio, we need $R_c \approx .05$. From the plot of breakdown voltage as a function of N_o [7] it is seen that one can use different combinations of N_o and Z to achieve a desired breakdown voltage. To determine, optimum values of N_o and Z, we make use of the results of Fig.(10) in conjuction with the above information. The optimum values of N_o and Z, thus obtained, are $N_o = 2.0 \times 10^{17}/cm^3$ and $Z = .17\,\mu$. The junction area 'A' of the diode is now calculated using the value of junction capacitance 'C_{25}' and plots of Fig.(13). The junction area calculated for the device is 6.0×10^{-4} cm^3 which corresponds to a circular area of approximate diameter 0.3 mm. In the above design, junction is assumed to be free of curvature effect which brings down the breakdown voltage [12]. The minimum epilayer thickness obtained from the plot of figure (13) is $1.4\,\mu$ and the corresponding cut off frequency 'fc_3' from Fig.(17) is 1.3×10^{11} Hz.

4.2 Fabrication Technology

The most widely used method of double diffusion was selected for the present work. The typical part of the fabrication process is to make the retrograded region which requires N_o of the order of $10^{17}/cm^3$. Conventional system employing open tube diffusion leads to surface concentrations order of magnitude larger than the required presently. For example, it is well known that owing to large segregation coefficient of phosphorus, it is difficult to get concentrations below $10^{19}/cm^3$ [10]. Several methods have been employed for achieving low surface concentrations. Amongst

these are: (a) Use of doped oxide source [1], (b) Drive-in of the impurities in a sealed ampule [6], (c) Etching out of the highly doped surface layer of diffused wafer to expose low concentration region [8], (d) Diffusion of impurities through an intermediate oxide layer [9] and(e) using commercially available low concentration preforms and spray-on films.

a) Limitations of Different Sources Used for Fabrication of Retrograded Region:

A simple and inexpensive method of achieving low surface concentration is by etching the highly doped surface layer of the substrate. Gupta et al have used this method for phosphorus diffused substrates. This method requires an accurate and uniform etching of the surface. A small difference in the etching rate can cause a large fluctuation in the value of N_o, especially in case of diffused wafers with a small value of characteristic length 'Z'. The method could be suitable for experimental investigation but may find restricted use in production due to problems of yield and large spread in device characteristics. Also, the method does not suit to the device fabrication using planar techniques.

Diffusion through intermediate oxide layers pose problems of reproducibility. Slight change in the density, quality or the thickness of the intervening oxide layer drastically affects the concentration at the silicon surface, particularly in case when

the concentration at the surface required is low.

Doped oxide source needs an elaborate set up and requires time to standarize the whole process. Though, the method is quite reliable, owing to time limitations was not employed for the present study.

The diffusion sources tried for the present study were low concentration phosphorus diffusant preforms (supplied by Transene Co) and diluted phosphorosilicafilm (supplied by Emulsitone Co.) besides initial trial with the $POCl_3$ system. $POCl_3$ system was abandoned in view of the limitations already pointed out at the beginning of this section. Instead, efforts were made to standardize the diffusion process using commercially available preforms and phosphorosilicafilm.

The diffusant preforms are thin film wafer diffusion sources for simplified and controlled diffusion processes. These preforms are meant to be sandwiched between the two silicon surfaces to be diffused. The lowest concentration which can be obtained on the diffused silicon surface using these preforms is $10^{18}/cm^3$ (phosphorus-1018N). The preforms are held by an organic binder which needs to be baked out, by the radiant heat at the mouth of the furnace, before pushing the boat into the furnace. The difficulty faced with these preforms was nonuniformity of the diffused layers. This nonuniformity could be seen on the surface of polished wafers clearly and was attributed to the warping of

the preform after the bake out. The weight of the wafer on the preform was inadequate to keep it flat during diffusion. Normally, these preforms are used with large stacks of silicon wafers which provide adequate weight to keep the intervening preforms flat. To overcome this difficulty a quartz piece was placed on the top of the wafers. After this step, the nonuniformity on the diffused wafer surface was not visible. However, when the wafers were etched to characterize the diffused layer, this nonuniformity showed up in the measurements as well as on the wafer surface. It was observed that when either the diffusion time or temperature was increased, this nonuniformity got reduced. This could be attributed to poor contact between the wafer and the preform on atomic scale. For deep diffusions, such as those used in high voltage rectifiers and PIN diodes, the effect gets smoothened out but for shallow diffusions that were needed in the present work, it remains quite pronounced. These preforms, therefore, were found unsuitable.

The source tried next was one using diluted phosphorosilica film. Different formulations, by mixing one drop of phosphorosilica film in varying volumes of undoped silicafilm were tried. High resistivity p-type silicon wafers were diffused after being coated with the above formulations. Sheet resistance of the diffused layer was measured using four-point probe. The junction depth was measured by angle-lapping and staining procedure. Concentration v/s

average resistivity curves [11] were used to determine the surface concentration assuming the distribution obtained to be erfc. A surface concentration of $5.0 \times 10^{17}/cm^3$ was obtained for a dopant film formulation of 1 drop of phosphorosilicafilm in 1 cc of silicafilm. This film was tried to obtain the desired device characteristics. The fabrication process is discussed in the next section.

b) Fabrication Process

Hyperabrupt $p^{+}n$ varicap diodes having MESA structure have been fabricated on n-type phosphorus doped nonepitaxial polished wafers. For the design calculations of section (4.1), the required background concentration 'N_B' was $1.0 \times 10^{16}/cm^3$ (for a given $N_o = 2.0 \times 10^{17}/cm^3$ & $R_c = .05$) which corresponds to a resistivity of 0.6 Ωcm. In order to determine the impurity distribution in the diffused layer, using diluted phosphorosilicafilm it was decided to use 3-7 Ω cm wafers for the initial runs. To achieve the characteristic length of .17 μ, diffusion time and temperature were calculated to be 90 minutes and 1100°C respectively [6]. The different fabrication steps are summarized as follows.

After following the normal acid and solvent cleaning, the diluted phosphorosilicafilm was spun on the polished side of the wafer at a speed of 3000 rpm for 10 seconds. This produces about 0.5 μ thin oxide layer. The film was hardened by baking the wafer at 200°C for half an hour in an oven. The wafer was

loaded on a quartz boat and moved slowly towards the flat-zone of the furnace at 1100°C. Oxygen & nitrogen flow rates during the diffusion were 200 cc/min and 500 cc/min, respectively.

After diffusion, the wafer was taken out and the oxide on the silicon surface was etched in 7% HF. The wafer was again loaded in the furnace alongwith activated BN wafer [13] to form the p^+ region. The furnace temperature during boron diffusion was 950°C and diffusion time was 20 minutes. Nitrogen flow rate during the diffusion was maintained at 500 cc/min. The wafer and the source were placed perpendicular to the direction of gas flow. Care was taken to ensure that the full wafer was exposed to the BN source. Any oxide formed on the surface of wafer during boron diffusion was etched in 7% HF. Stray diffusion from the back of the wafer was etched in 1:5:1 (1 HF, 5HNO_3, 1 Acetic acid) etchant [22] after protecting the front surface by a thick layer of apiezon wax.

Nickel was deposited on the back surface by electroless Nickel solution (Ammonia Type) [14]. After proper cleaning of the wafer Cr and Au were evaporated on the front side of the wafer at a pressure of 2×10^{-5} torr. Cr-layer was kept very thin (of the order of 100 Å) and substrate was heated, using a substrate holder, to about 200°C. Cr-evaporation was immediately followed by Au evaporation using another filament in the same vacuum chamber.

To etch MESA's of well defined geometry, an available photolithography mask of 0.4 mm diameter was used. Mixture of KMER and thinner (1:1 by volume) was spun over the wafer at a speed of 6000 rpm for 10 seconds. The film was prebaked in oven at a temperature of 90°C for 15 minutes and then exposed to ultraviolet light through the mask for 20 seconds. Next, the wafer was developed in Kodak Thin Film Developer for two minutes and then put in the Rinse to remove all the traces of developer. After rinse, the wafer was dried and post baked in oven at a temperature of 160°C for 30 minutes. After protecting the back nickel by a coating of black wax , the unprotected gold film on the front side was etched in gold-etchant solution [ ] and the chromium layer thus exposed was etched in ferricyanide etch. (see Appendix for etchant formula). The wafer was then put in 1:5:1 [22] etching soln. for two minutes to etch the MESA's. The etching rate of this solution was measured to be 12 μ/min. The expected MESA height was about a mil. The photoresist from the dots was removed by boiling the wafers in stripper. Black wax from the back was also removed by boiling the wafer in TCE. Cr-Au evaporation was done to make use of the photolithography process to get devices of well defined geometry . Gold was used becuase it can withstand the etchant, and Cr-layer was sandwiched to improve adhesion of the gold film to silicon.

4.3 Measurements

Out of a number of devices made on the wafer, about 20% of them showed a sharp breakdown above 25 volts. The breakdown voltage of the devices were determined directly from the display of I-V characteristics on the curve tracer. Out of the lot, three representative devices were selected for the study of their C-V characteristics.

The capacitance measurements were performed on a Boonton capacitance bridge, Type 74C-S18 at a fixed internal frequency of 100 kc/s. The corresponding voltage was measured using a digital voltmeter(Yamuna make). The observed C-V relations for one of the devices is shown in Fig.(22). Impurity concentration in the retrograded region was determined (assuming the junction to be one sided) from the slope of the $1/C^2$ v/s V_a curve of fig.(23) at a number of points, using equations (17) and (18) of chapter III.

The doping profile of the device, thus obtained, is shown in figure (24). The representative devices had a leakage current of less than 1.0 μ at 25 volt.

4.4 Results and Discussion

From the concentration v/s distance graph of Fig.(24), it is seen that the extrapolated value of N_o is $2.2 \times 10^{16}/cm^3$ which is an order of magnitude less than the desired value of $2 \times 10^{17}/cm^3$. The value of 'Z' determined from the same plot is

.15 μ, which is not far removed from the designed value of .17 μ. Series resistance estimated from the forward characteristics is around 100 ohms. The built-in voltage of the junction obtained from $\frac{1}{C^2}$ vs V_a plot is about 0.5V .

The low value of 'N_o' obtained in this run, could be primarily due to deeper diffusion of the p^+ layer using boron nitride source and secondly due to variation in the formulation of diluted phosphorosilicafilm. The low value of built-in voltage suggests that the junction formed is graded instead of an abrupt one, and the doping profile of Fig.(24), only represents the equivalent one-sided structure of the actual device. This also causes a reduction in the value of N_o. The high value of series resistance of the device is due to use of nonepitaxial wafer. Contact resistance of nickel on 3-7 Ω-cm wafer is reported to be of the same order [17].

The background resistivity of the junction is calculated to be $1.0 \times 10^{15}/cm^3$ which corresponds to a resistivity of 5 Ω-cm and is within the specified resistivity range (3-7Ω-cm) of the wafer.

From the plot of figure (24), it can be seen that the retrograded region of the device is almost swept at 3 volts and the junction starts behaving like an abrupt junction. In the voltage range of 3 to 25 volts, hyperabrupt nature of the device is lost, and the capacitance ratio obtained is 3.5, instead of the

proposed value of 6. Capacitance ratio for an equivalent abrupt junction is 2.8. Further work is in progress to take care of the various limitations.

CHAPTER V

CONCLUSION

Design plots have been developed which can be used to obtain the optimum profile parameters N_o, R_c and z for a one-sided hyperabrupt varicap with exponentially doped retrograded region. Built-in voltage of the junctions has been computed for various values of N_o, R_c and Z. Capacitance ratio 'C_3/C_{25}' has been calculated for all the above combinations of N_o, R_c and Z, utilising the knowledge of the built-in voltage. The built in voltage is also needed to find out the exact value of applied voltage corresponding to 'n_{max}' [18].

Some interesting results have been obtained from the plots of capacitance ratio v/s the concentration N_o. It is observed that, for a given 'Z', maximum of 'C_3/C_{25}' always occurs at the same value of 'N_o' for different values of 'R_c', and the value of this maximum is independent of 'Z' for a given 'R_c'. To achieve the $(C_3/C_{25})_{max}$ it is seen that the value of log Z decreases linearly with a logarithmic increase in the value of N_o. Similarly, there is a linear decrease in the logarithmic value of $(C_3/C_{25})_{max}$ with increasing log R_c. These two plots, in conjuction with the breakdown voltage curves [7] are sufficient to determine the values of N_o, R_c and Z for a given design.

Graphs of minimum required epilayer thickness have been obtained for the above mentioned values of N_o, R_c and Z. Cutoff frequency 'fc_3' of the varicap has been calculated assuming minimum epilayer thickness. This frequency sets the upper limit to the cutoff frequency, because all the stray contributions, viz., resistance of the substrate, contact resistance, encapsulation capacitance etc., have been neglected.

Using the above information, a design of a varicap for use in the VHF range has been worked out. Various diffusion sources tried for the fabrication of retrograded region are phosphorus oxychloride, n-type low concentration diffusant preforms and diluted phosphorosilicafilm. After abondoning the first two, diluted phosphorosilicafilm has been utilised for the fabrication of the device. A device with MESA structure has been fabricated using photolithography on Cr-Au layers evaporated on diffused wafers. Though, the desired surface concentration could not be achieved due to nonavailability of a proper diffusion source, the results obtained are in conformity with the results of our calculations.

The diluted phosphorosilicafilm acts similar to a doped oxide source. Therefore, if one utilises standard formulations of low concentration phosphorosilicafilm (supplied by Emulsitone Company, USA), it should obviate the need of developing a set-

up for the doped-oxide source saving much of the time which is needed to standardize the process.

One easy way of fabricating the retrograded region with high values of R_c ($>.1$) and low values of 'Z' could be by oxidation of a substrate (with background concentration N_B) in steam at low temperature (around 800°C to 900°C). In this method, silicon at the surface of the wafer is consumed in making silicon dioxide and the dopant present in this layer accumulates at the $Si-SiO_2$ interface, being rejected by the grown oxide. The concentration rise at the surface is determined only by the temperature of the oxidation [19]. This rise in the surface concentration is independent of time because both, the rate of accumulation of the dopant at the interface (determined by the rate of oxidation) and the rate of diffusion of the dopant into the silicon, have square-root dependence on time and, therefore, cancel out. With increasing time, only the diffusion length (or characteristic length) increases. This method provides a way by which both R_c and Z could be controlled independently. Since, the value of 'R_c' required in the present case, was .05, this method could not be employed for the present study.

APPENDIX

1. Composition of gold-etchant:

125 cc Distilled Deionised Water

14 gms. Iodine

28 gms. Pot. Iodide

2. Composition of Ferricyanide etch:

Solution A

50 cc Distilled Deionised Water

25 gm. Sodium hydroxide

Solution B

150 cc Distilled Deionized Water

50 gm. Pot. Ferricyanide

Solution A and Solution B are mixed in a ratio of 1:3.

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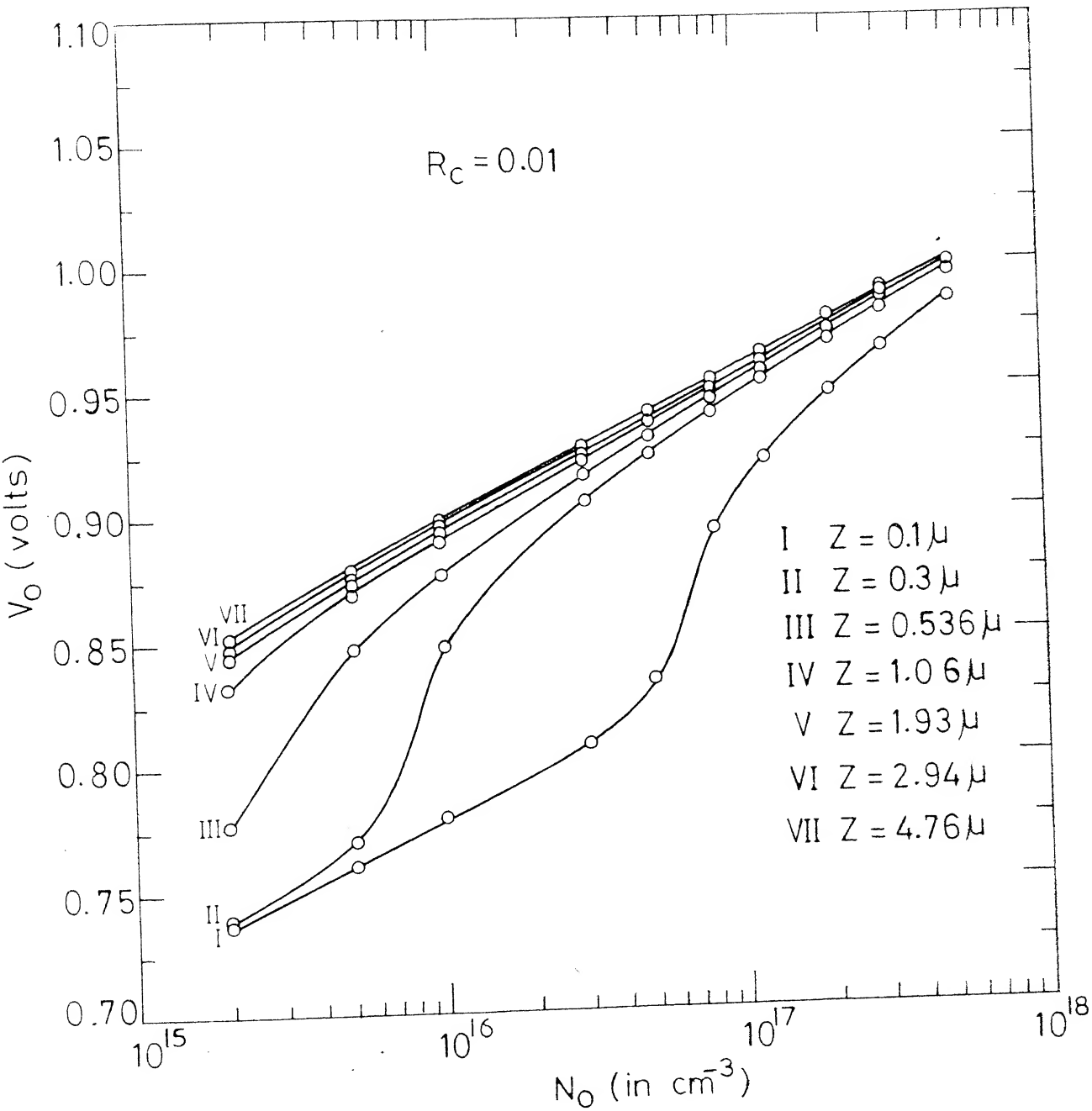
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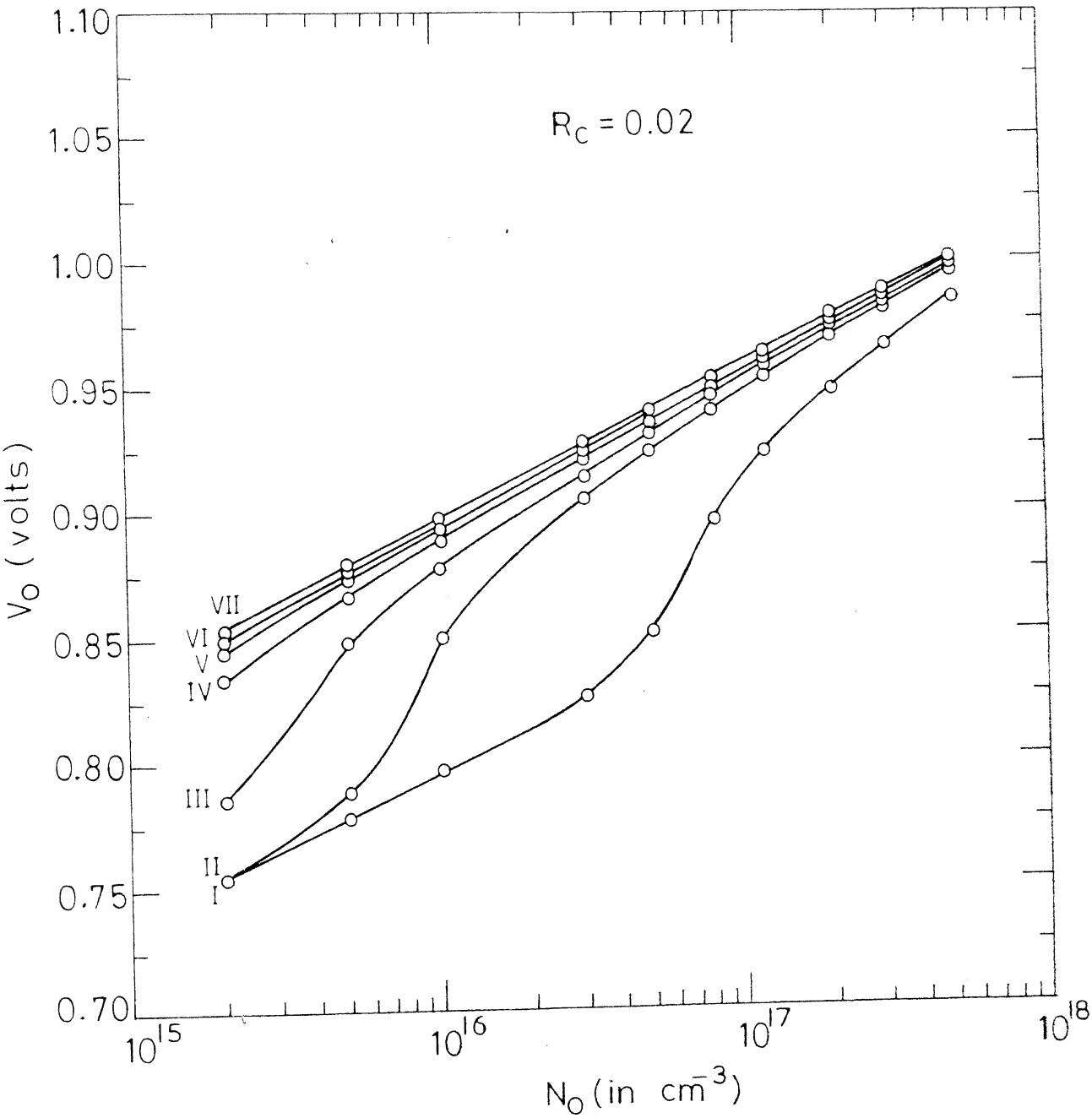
1.05
1.00
0.95
0.90
0.85
0.80
0.75
0.70
V_o (volts)
$R_c = 0.01$
I Z = 0.1 μ
II Z = 0.3 μ
III Z = 0.536 μ
IV Z = 1.06 μ
V Z = 1.93 μ
VI Z = 2.94 μ
VII Z = 4.76 μ
VII
VI
V
IV
III
II
I
10^{15}
10^{16}
10^{17}
10^{18}
N_o (in cm^{-3})

Fig. 2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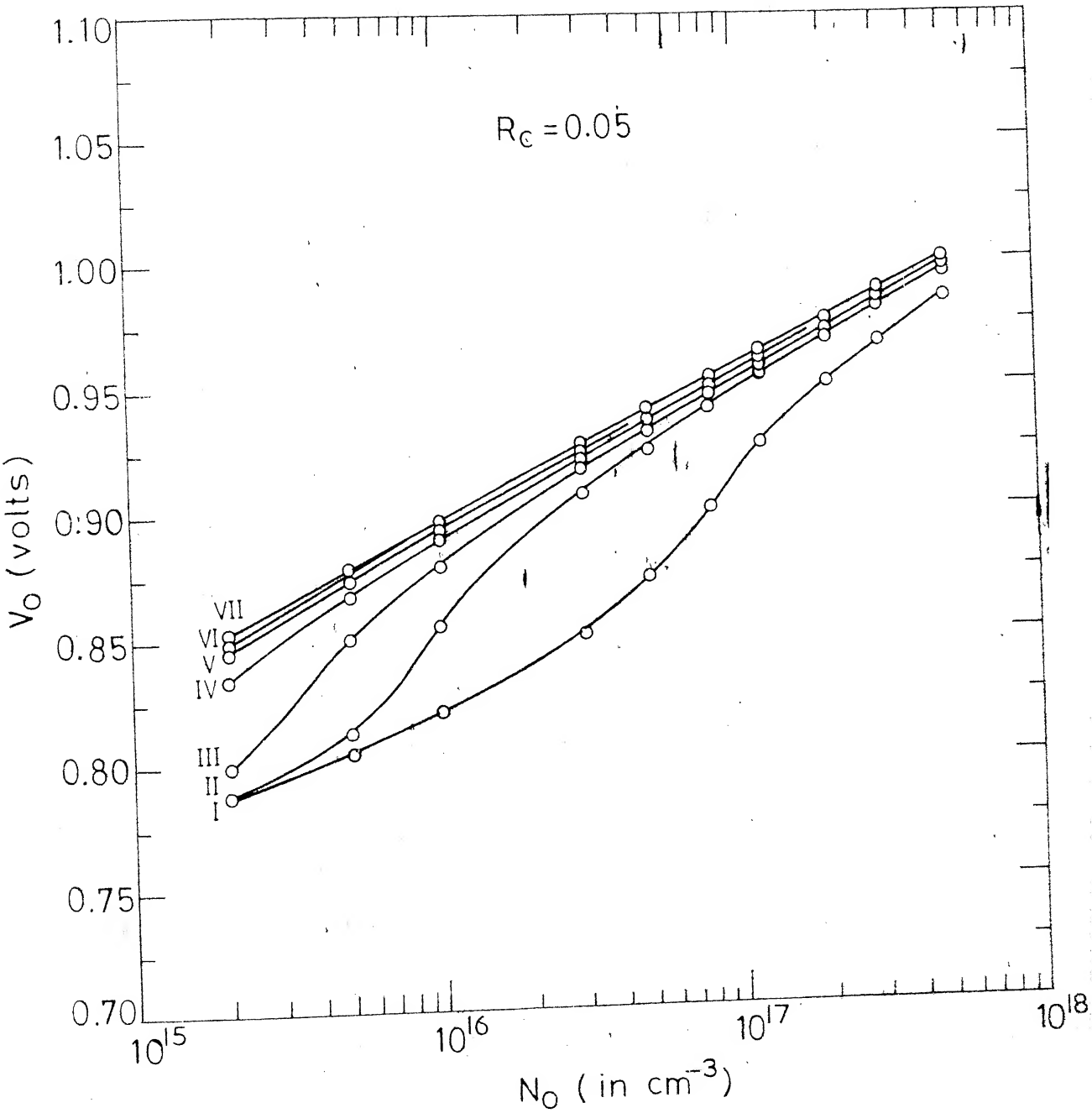
1.05
1.00
0.95
0.90
0.85
0.80
0.75
0.70
V_o (volts)
$R_c = 0.02$
VII
VI
V
IV
III
II
I
10^{15}
10^{16}
10^{17}
10^{18}
N_o (in cm^{-3})

Fig. 3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V_o (volts)
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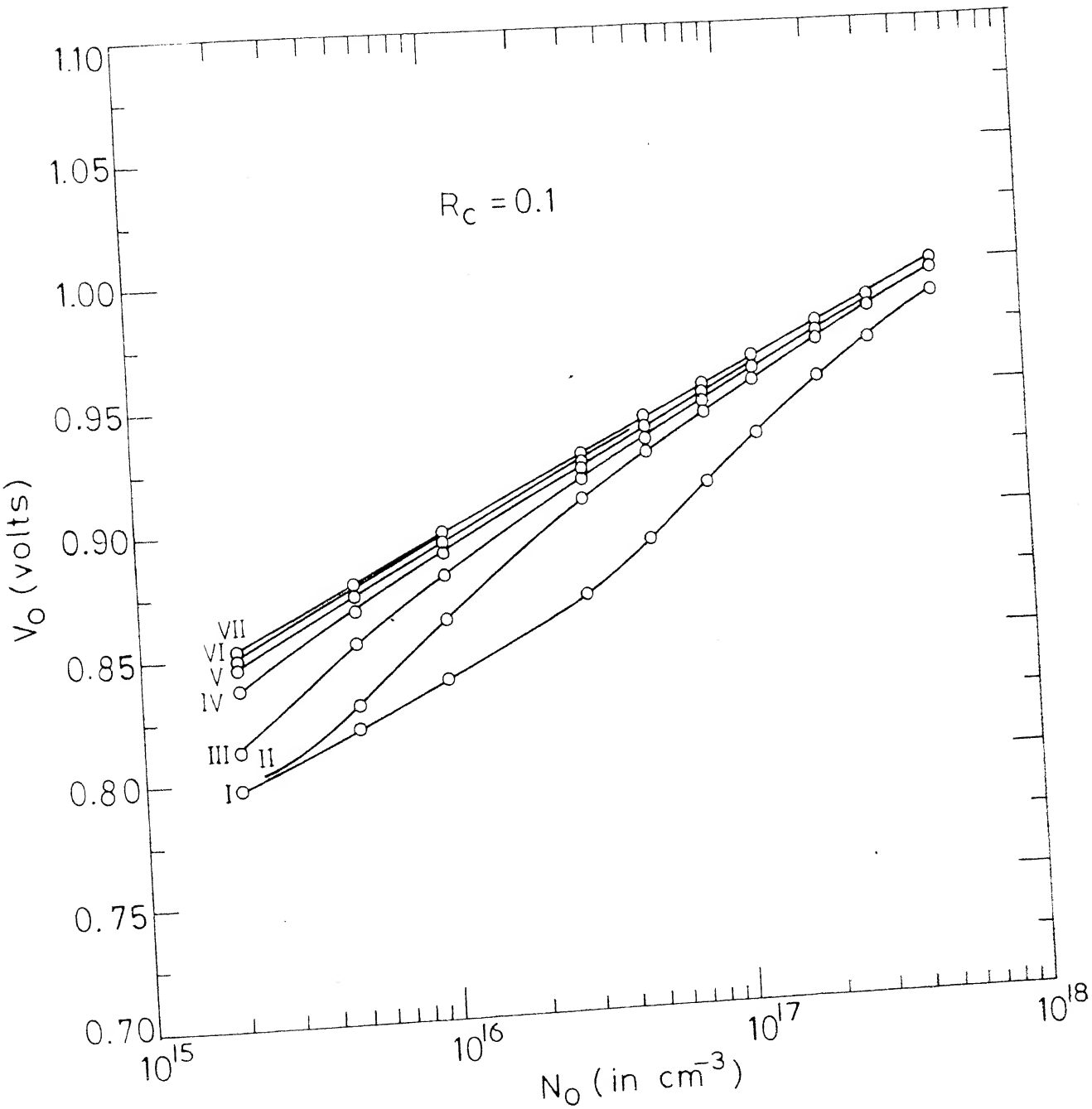
1.05
1.00
0.95
0.90
0.85
0.80
0.75
0.70
VII
VI
V
IV
III
II
I
10^{15}
10^{16}
10^{17}
10^{18}
N_o (in cm^{-3})

Fig. 4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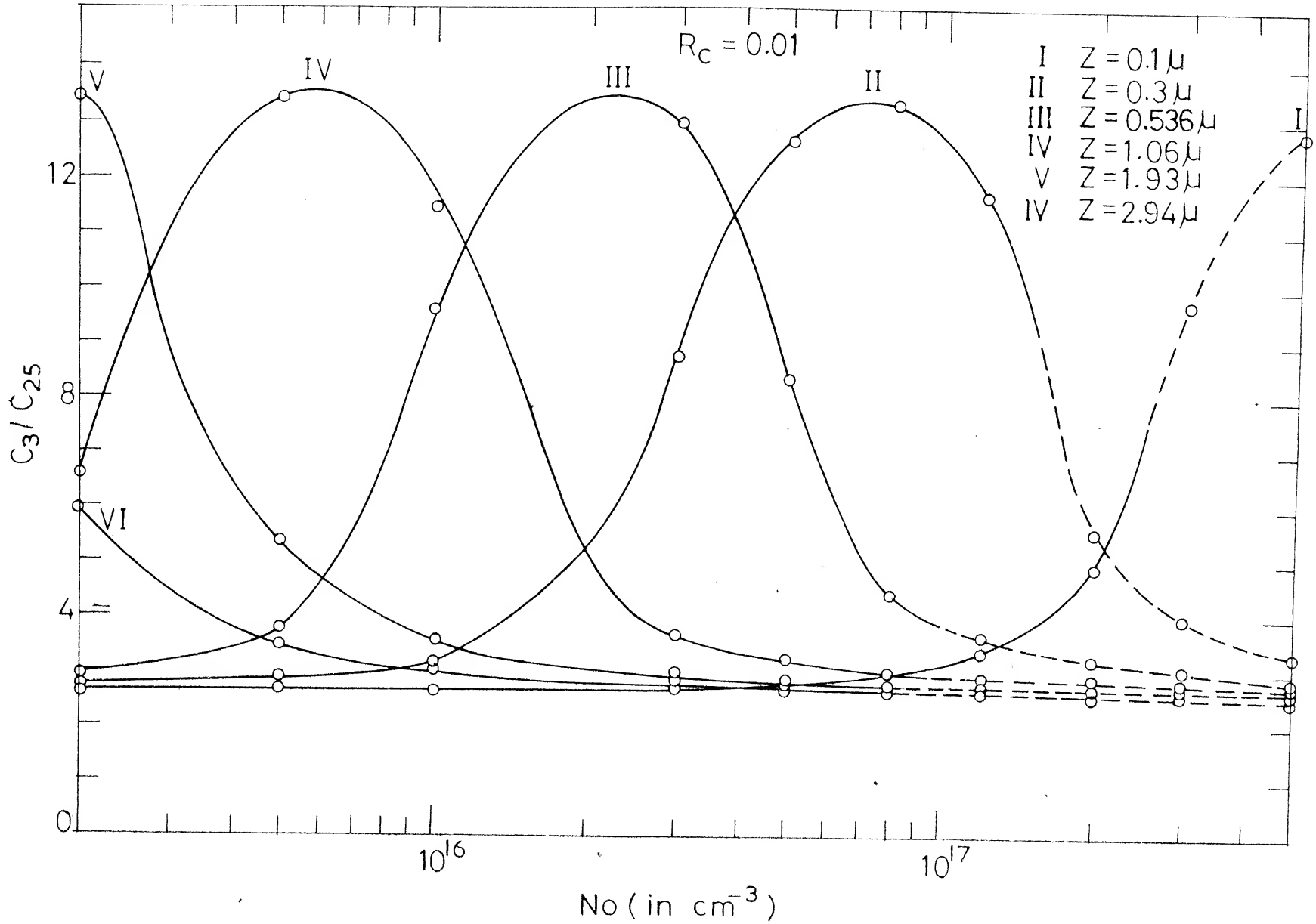
1.05
1.00
0.95
0.90
0.85
0.80
0.75
0.70
V_o (volts)
$R_c = 0.1$
VII
VI
V
IV
III
II
I
10^{15}
10^{16}
10^{17}
10^{18}
N_o (in cm^{-3})

Fig. 5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I Z = 0.1 μ
II Z = 0.3 μ
III Z = 0.536 μ
IV Z = 1.06 μ
V Z = 1.93 μ
IV Z = 2.94 μ
V
IV
III
II
I
VI
12
8
4
0
C_3 / C_{25}
10^{16}
10^{17}
No (in cm^{-3})

Fig. 6

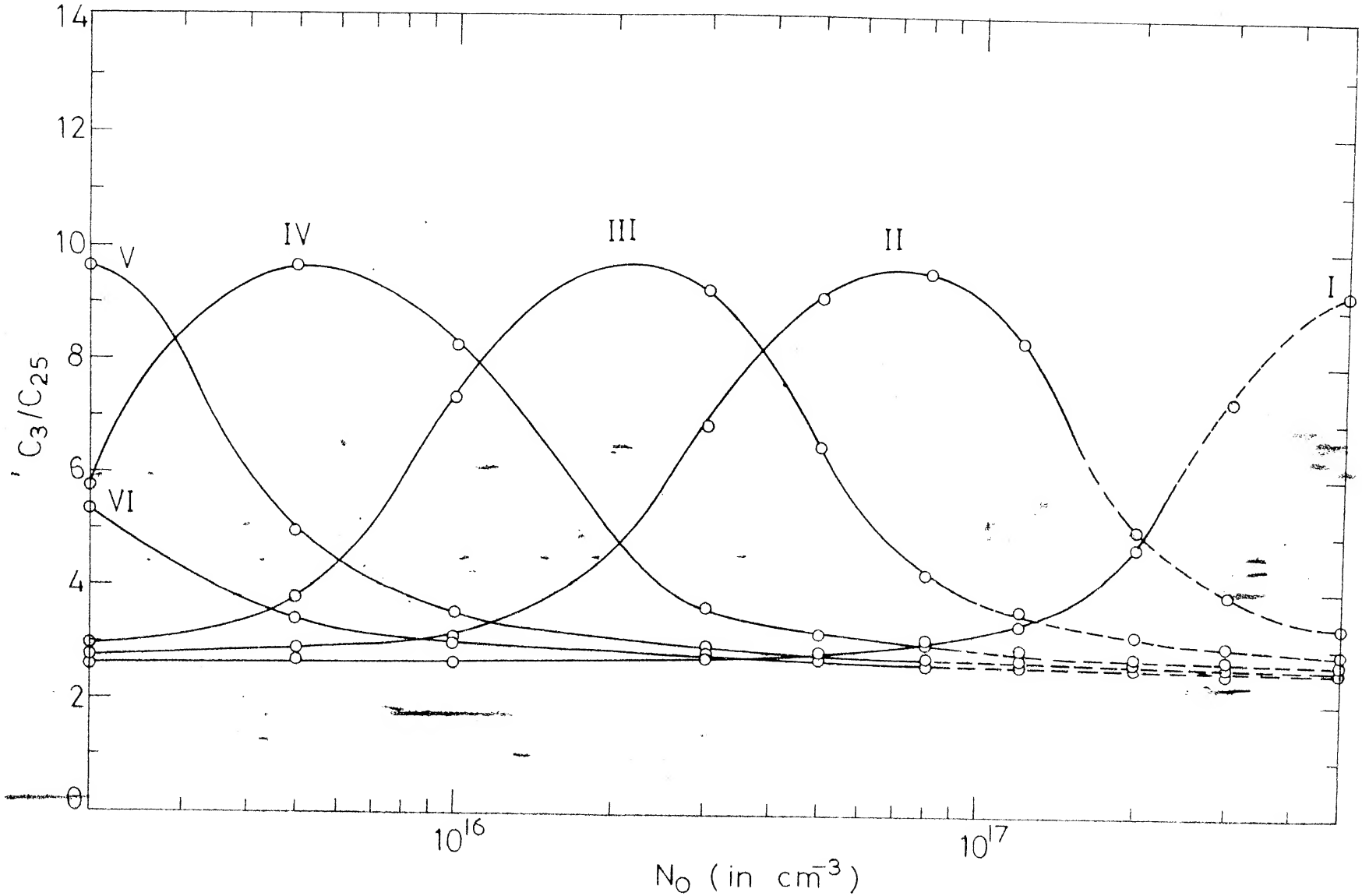

Fig. 7

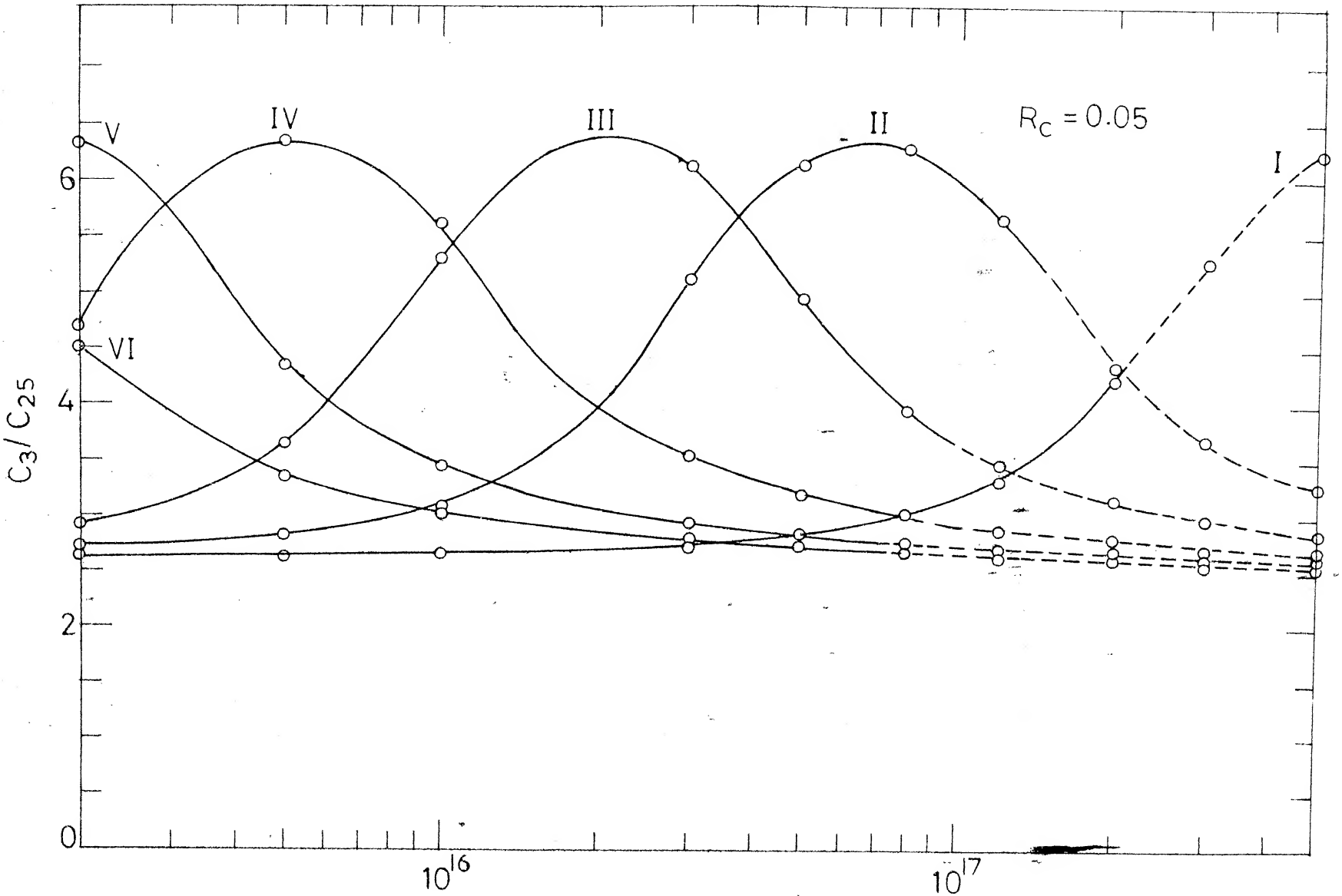

Fig. 8

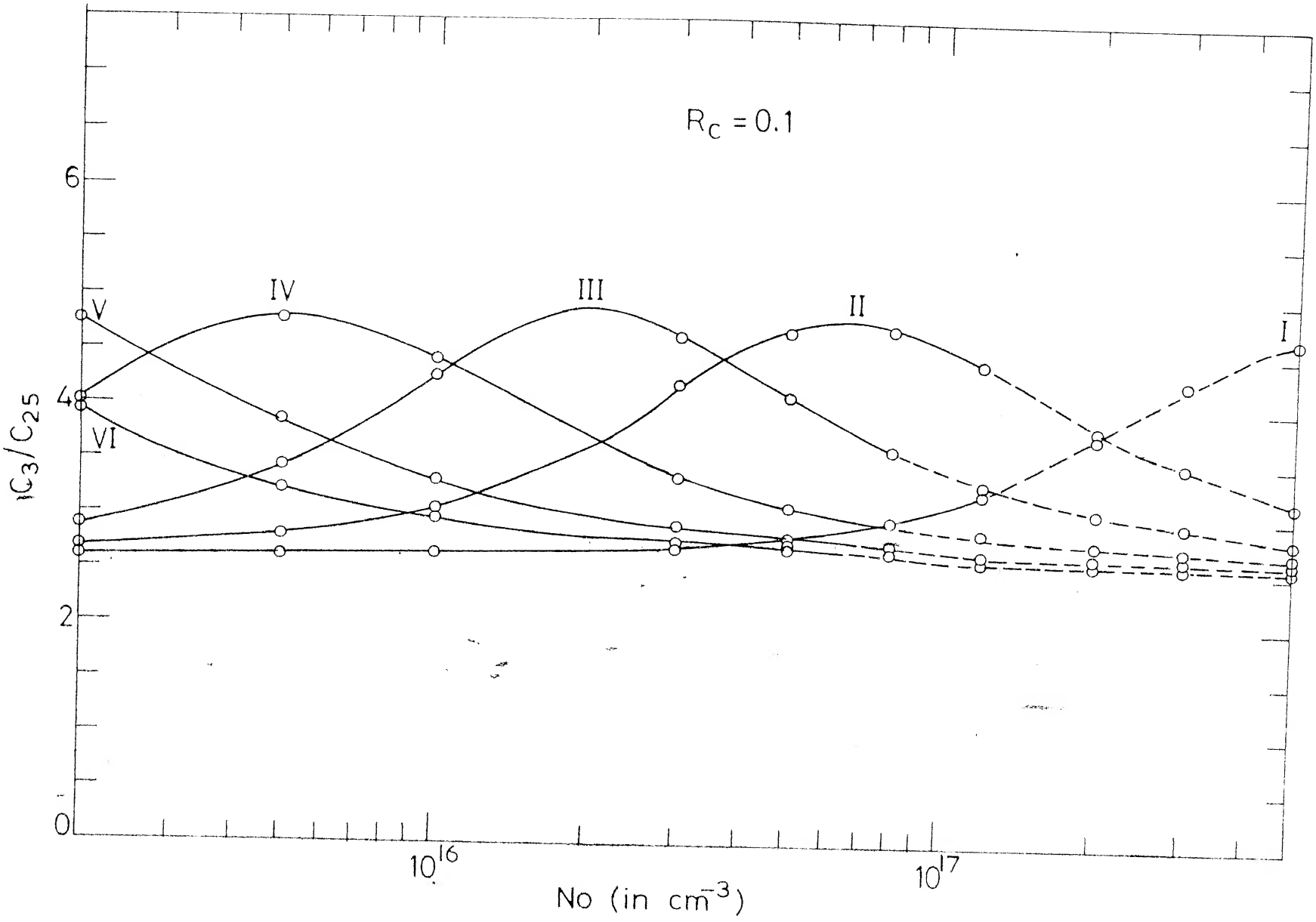

Fig 9

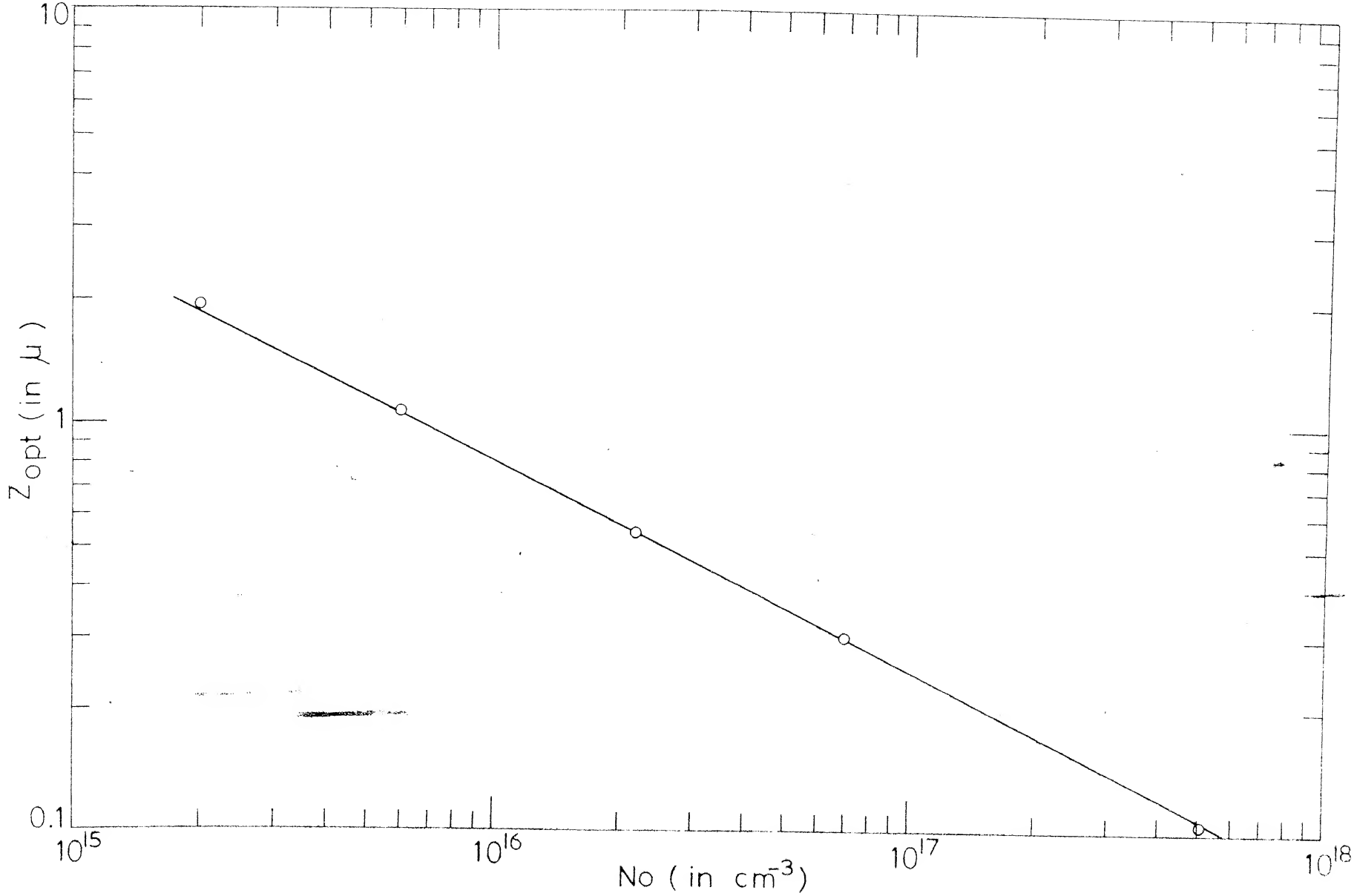

Fig. 10

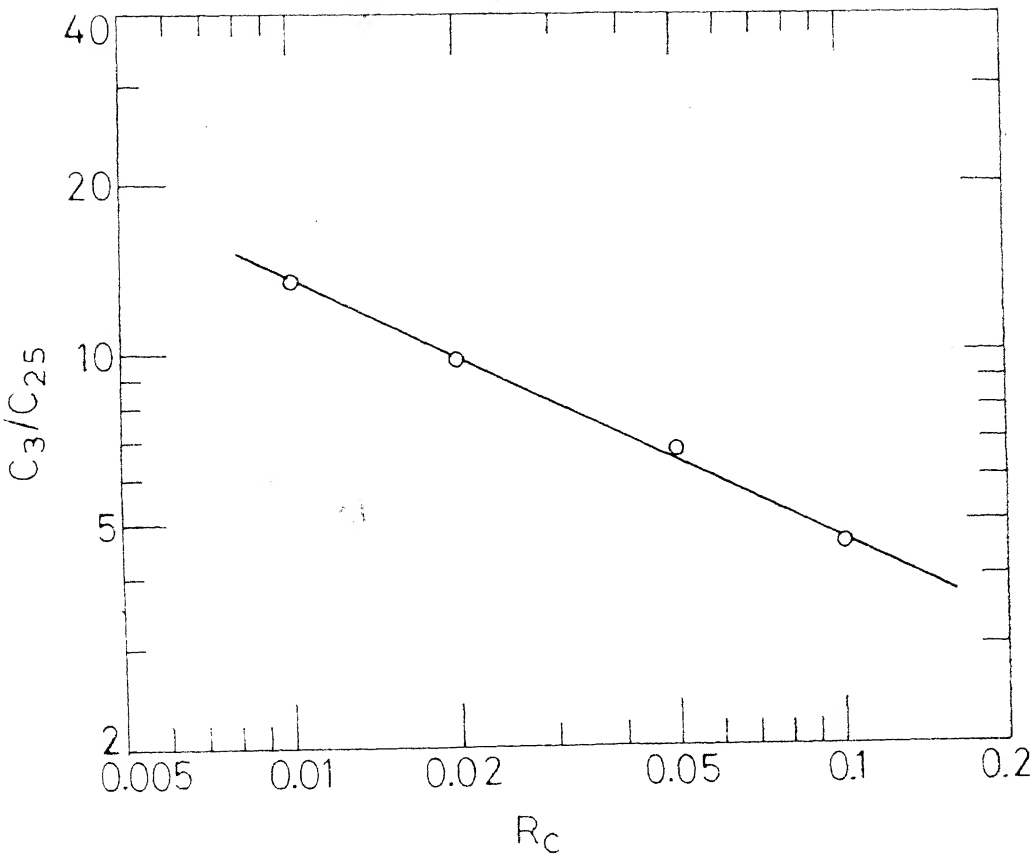

Fig. 10(a)

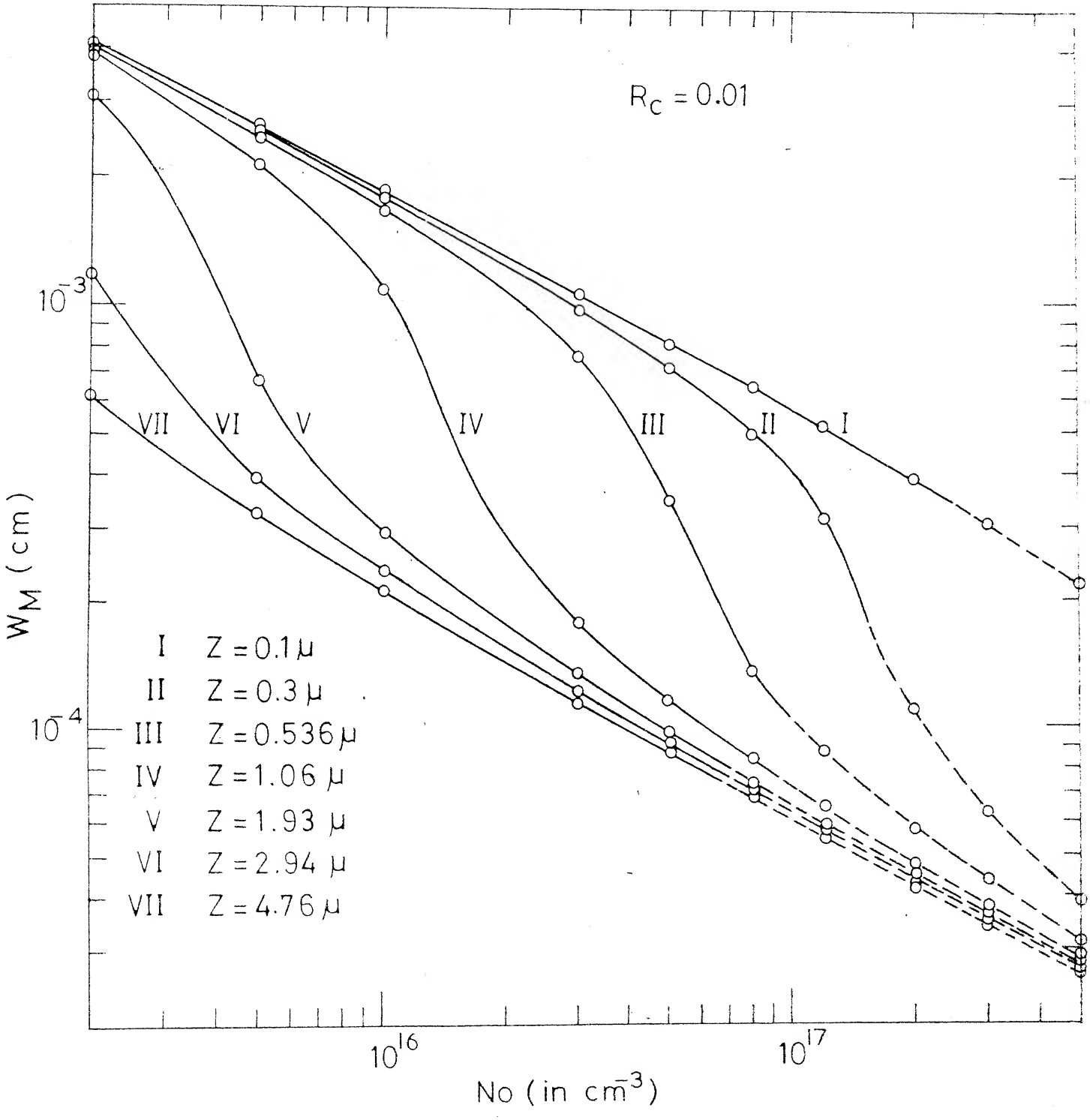
$R_C = 0.01$
10^{-3}
10^{-4}
W_M (cm)
VII
VI
V
IV
III
II
I
I Z = 0.1 μ
II Z = 0.3 μ
III Z = 0.536 μ
IV Z = 1.06 μ
V Z = 1.93 μ
VI Z = 2.94 μ
VII Z = 4.76 μ
10^{16}
10^{17}
No (in cm^{-3})

Fig. 11

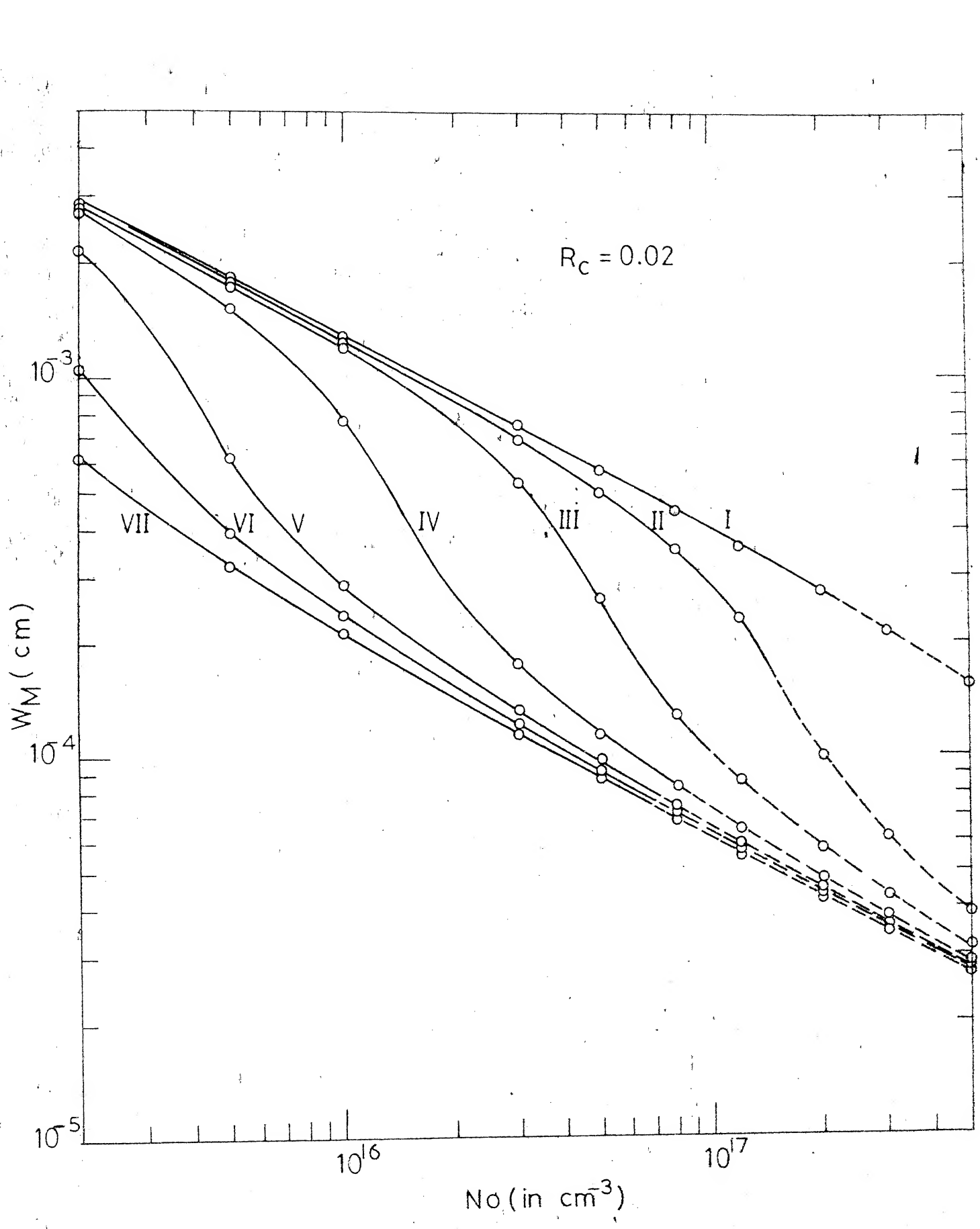

Fig. 12

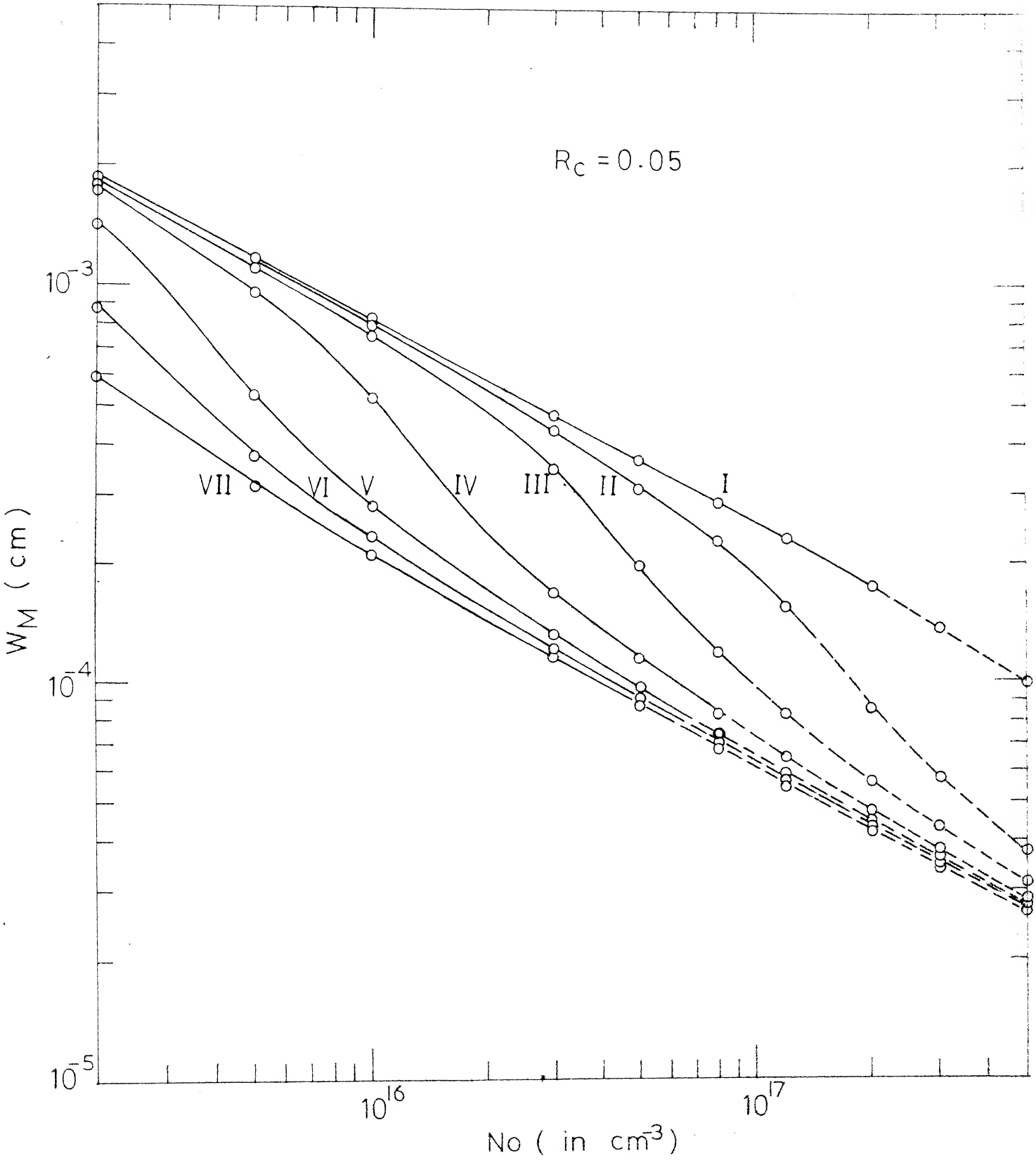

Fig. 13

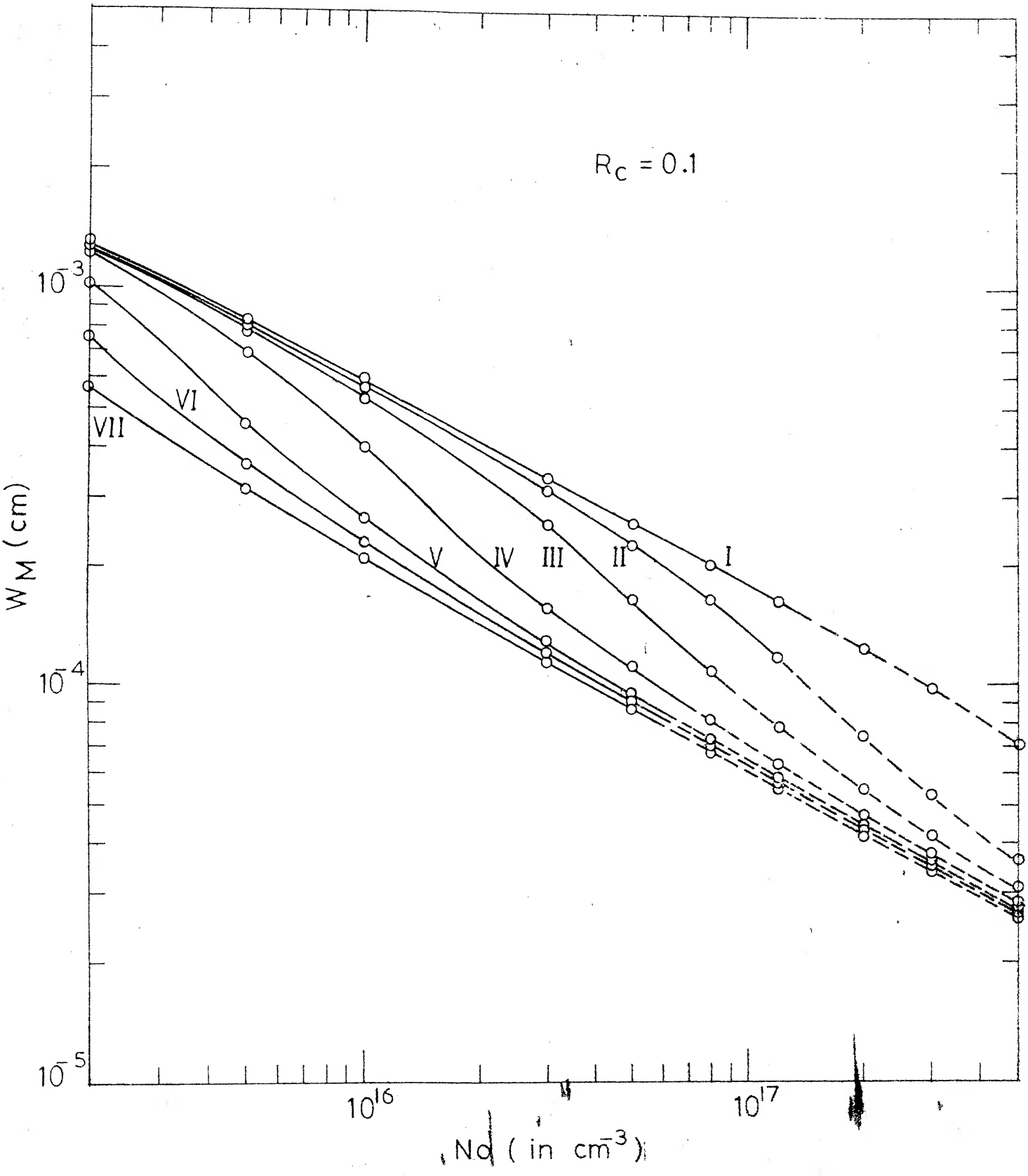

Fig. 14

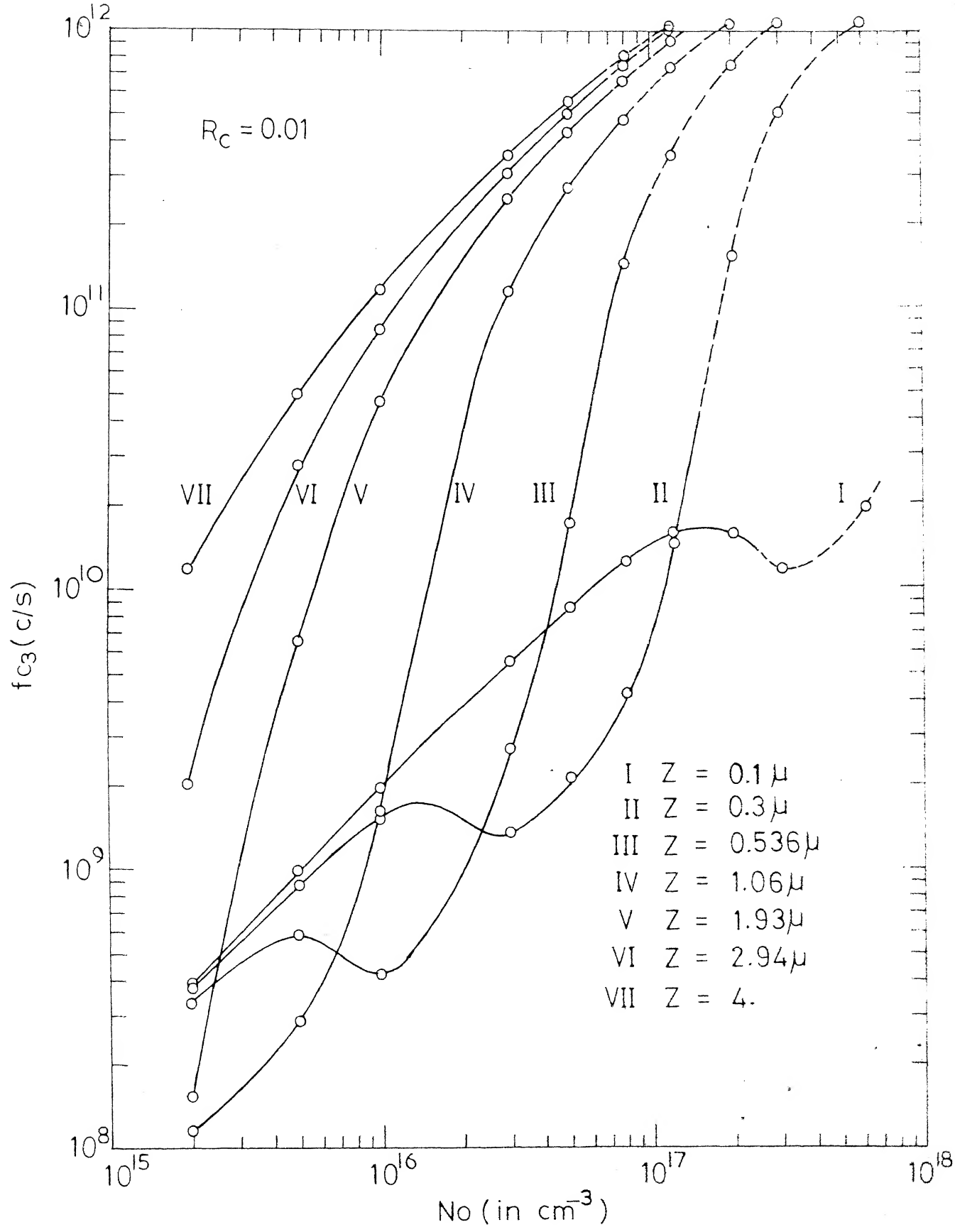
10^{12}
10^{11}
10^{10}
10^{9}
10^{8}
f_{C_3} (c/s)
$R_C = 0.01$
VII
VI
V
IV
III
II
I
I Z = 0.1 μ
II Z = 0.3 μ
III Z = 0.536 μ
IV Z = 1.06 μ
V Z = 1.93 μ
VI Z = 2.94 μ
VII Z = 4.
10^{15}
10^{16}
10^{17}
10^{18}
No (in cm^{-3})

Fig. 15

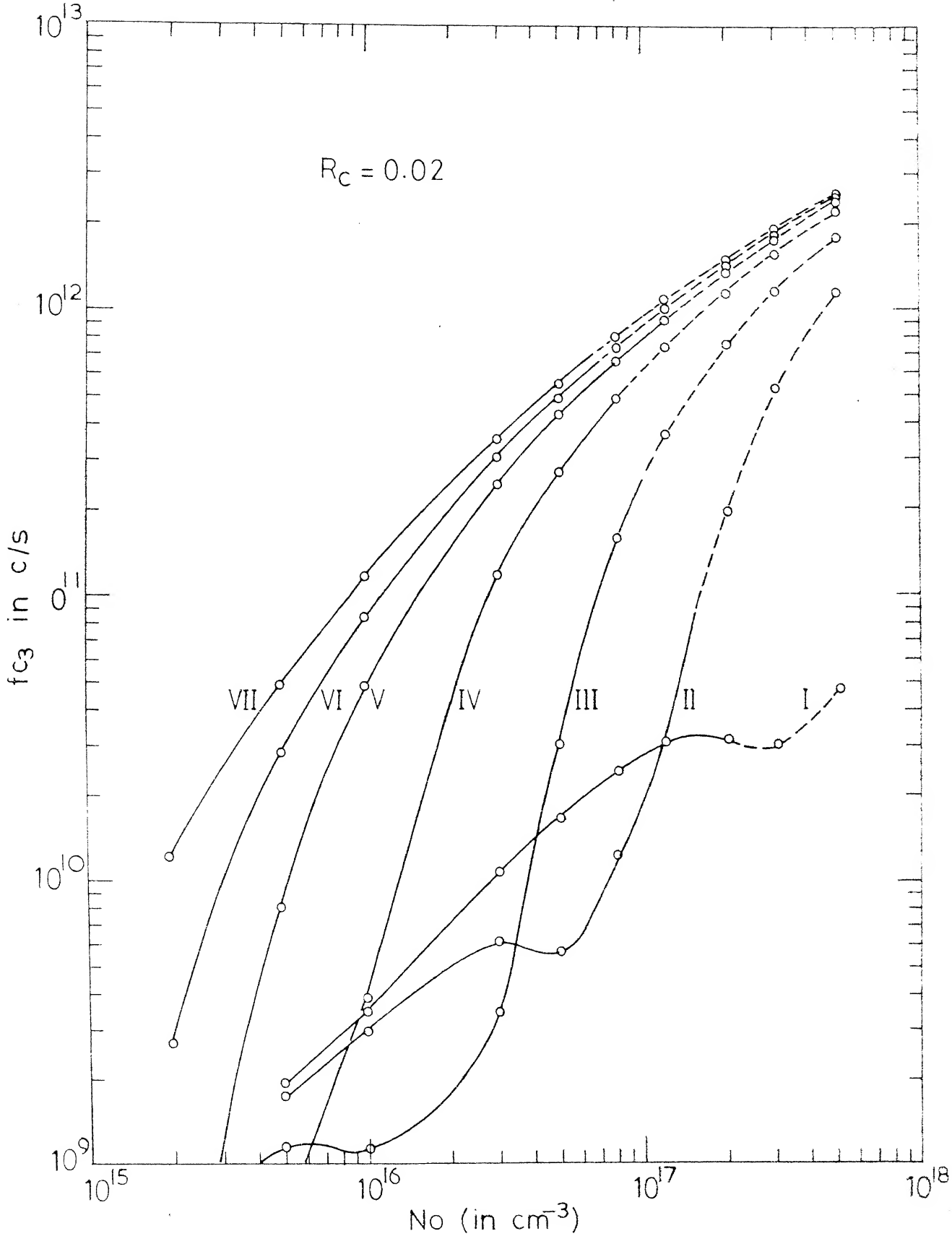
10^{13}
10^{12}
10^{11}
10^{10}
10^{9}
$R_c = 0.02$
f_{c_3} in c/s
VII
VI
V
IV
III
II
I
10^{15}
10^{16}
10^{17}
10^{18}
No (in cm^{-3})

Fig.16

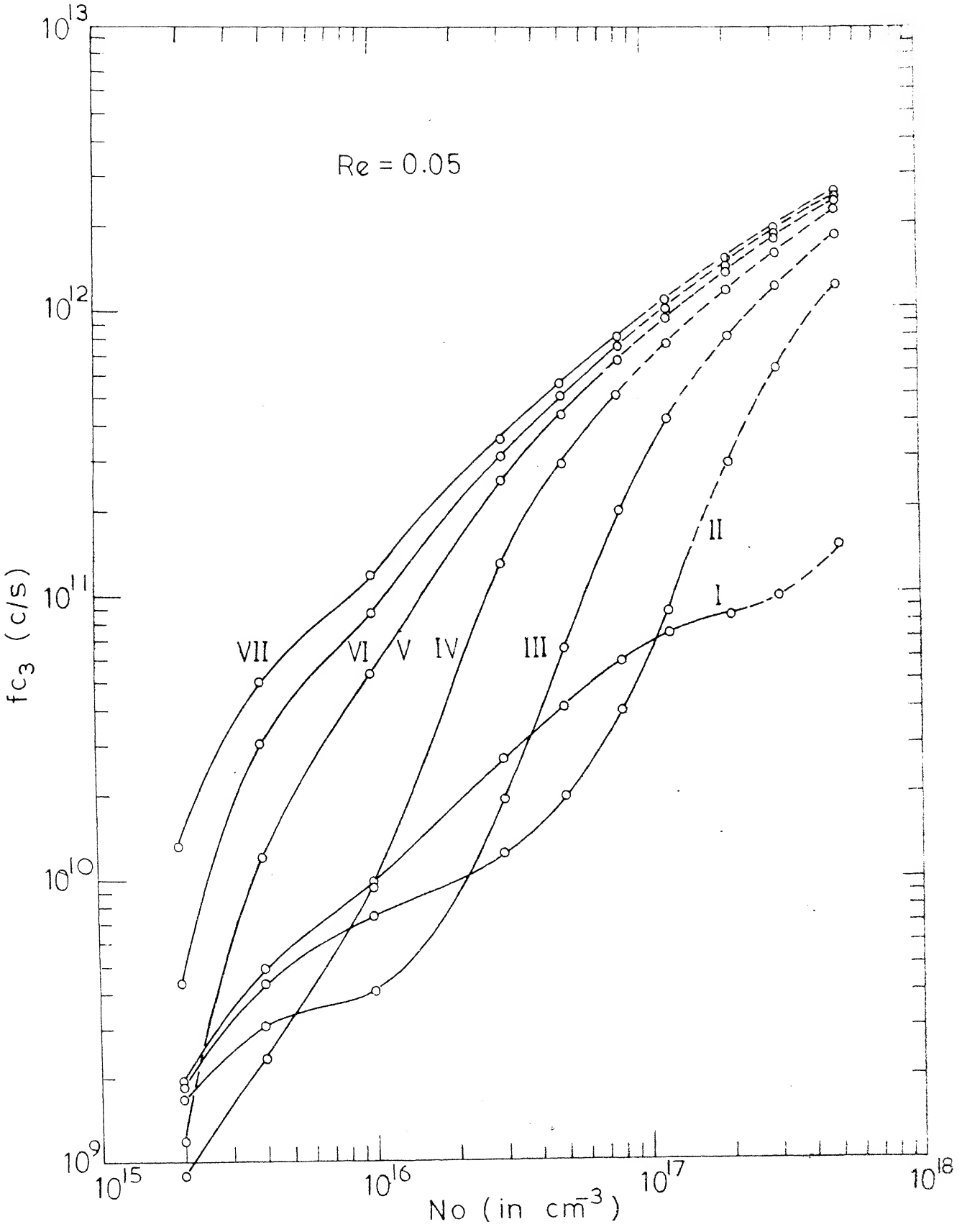
Re = 0.05
10^{13}
10^{12}
10^{11}
10^{10}
10^{9}
fc_3 (c/s)
VII
VI
V
IV
III
II
I
10^{15}
10^{16}
10^{17}
10^{18}
No (in cm^{-3})

Fig.17

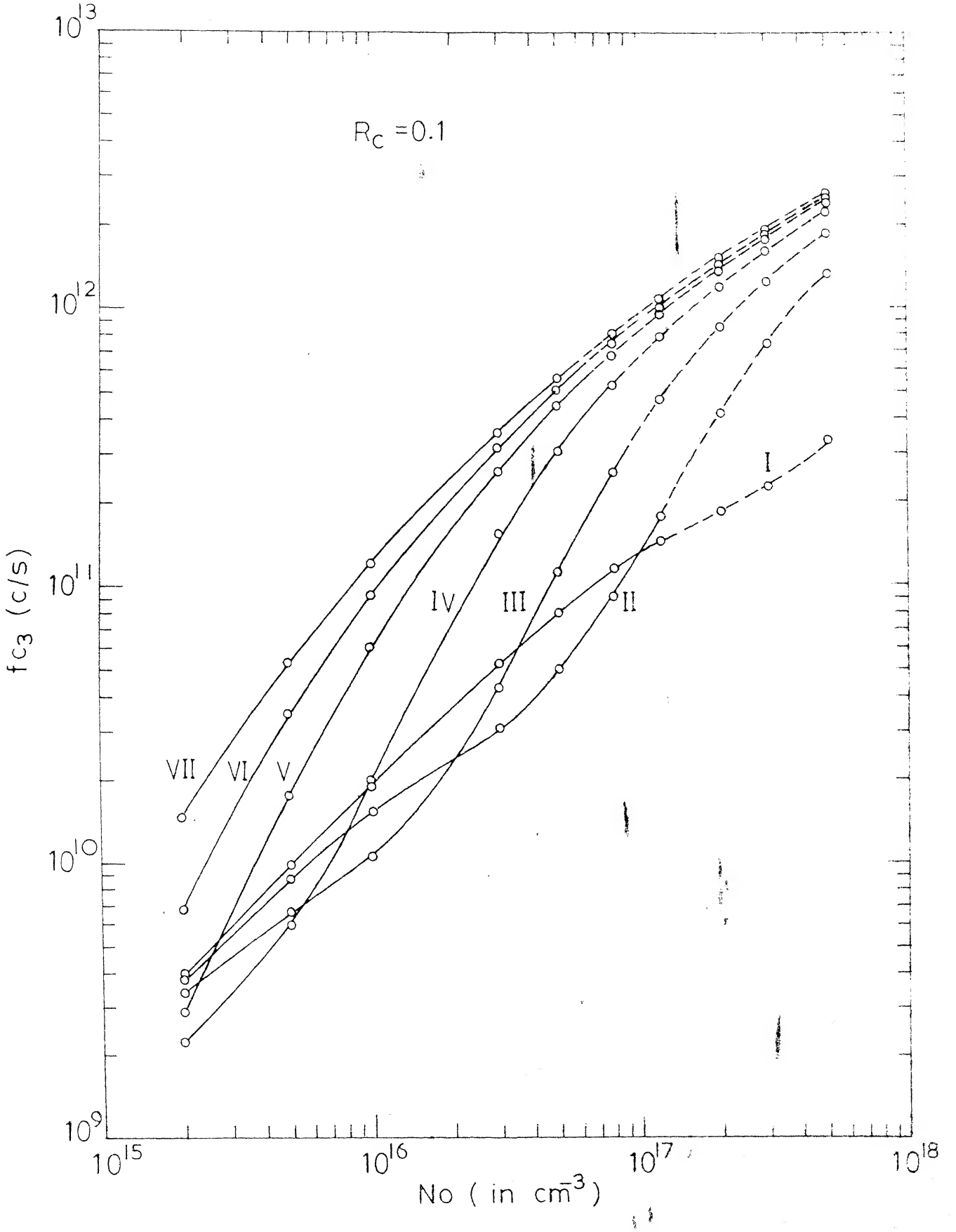
10^{13}
10^{12}
10^{11}
10^{10}
10^{9}
R_c =0.1
f_{c_3} (c/s)
VII
VI
V
IV
III
II
I
10^{15}
10^{16}
10^{17}
10^{18}
No (in cm^{-3})

Fig.18

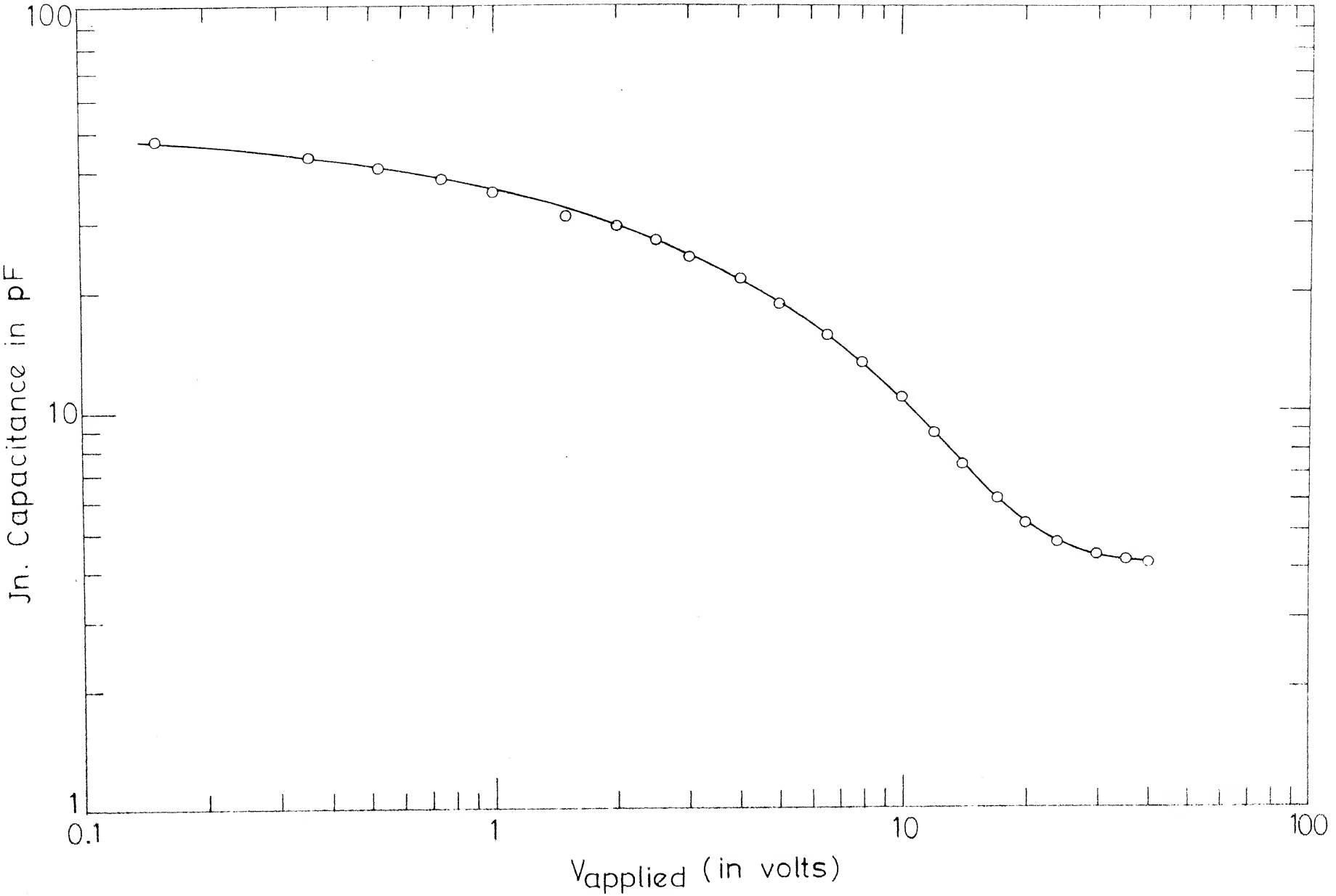

Fig. 1·9

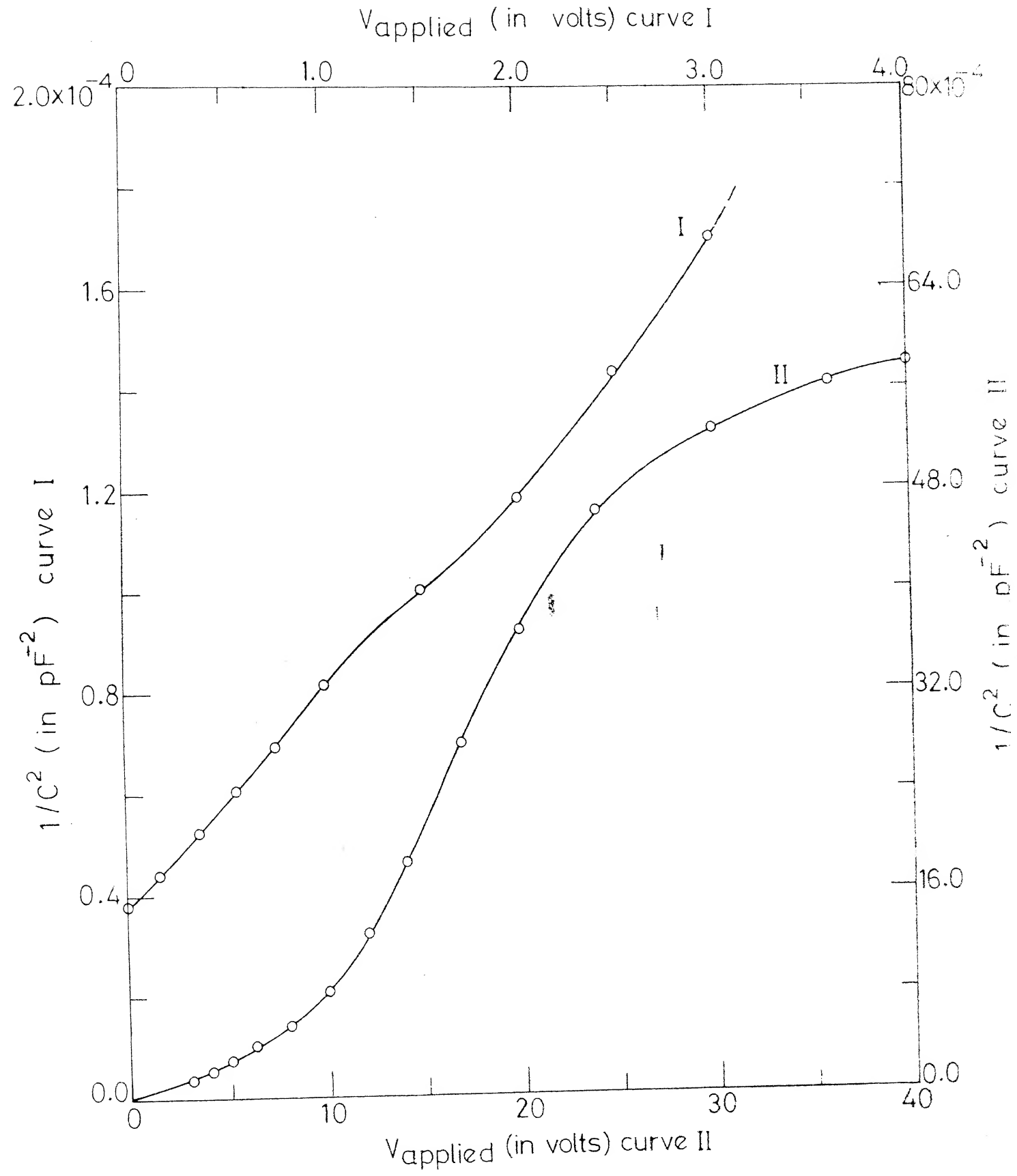
Vapplied (in volts) curve I
0
1.0
2.0
3.0
4.0
2.0x10⁻⁴
80x10⁻⁴
I
II
1.6
1.2
0.8
0.4
0.0
64.0
48.0
32.0
16.0
0.0
1/C² (in pF⁻²) curve I
1/C² (in pF⁻²) curve II
0
10
20
30
40
Vapplied (in volts) curve II

Fig. 20

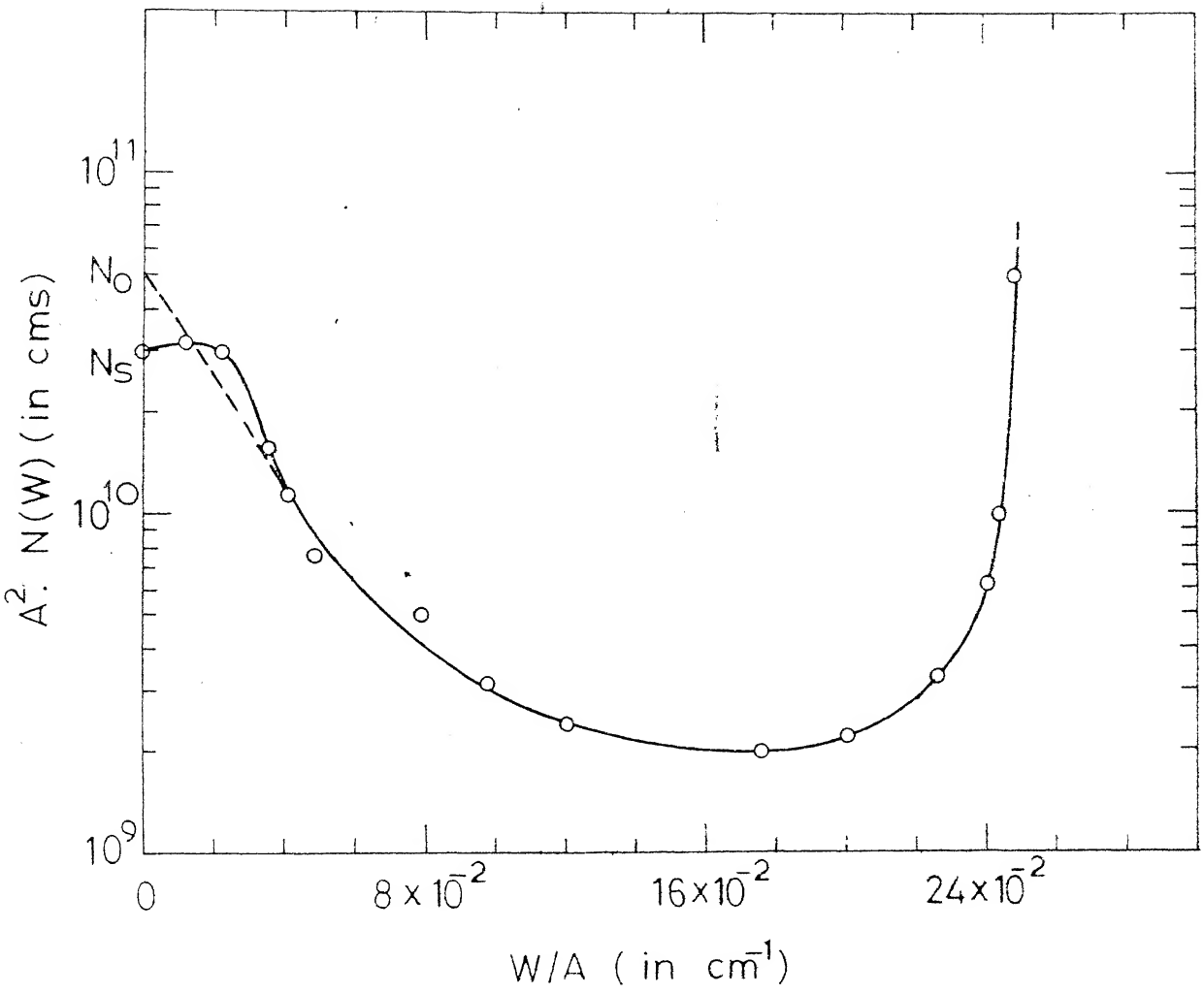
10^{11}
N_O
N_S
10^{10}
10^9
A^2. N(W) (in cms)
0
8×10^{-2}
16×10^{-2}
24×10^{-2}
W/A (in cm^{-1})

Fig. 21

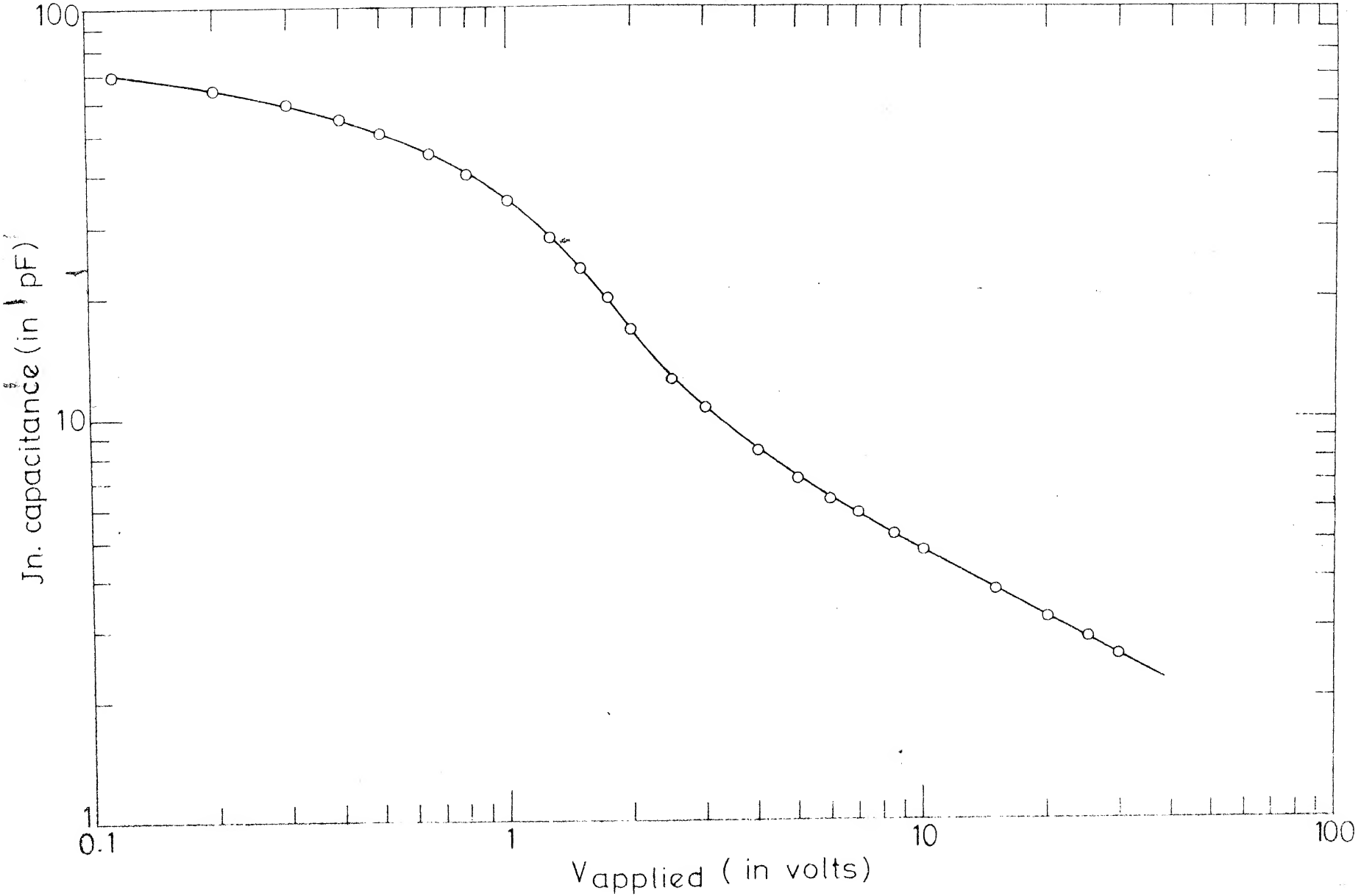

Fig. 22

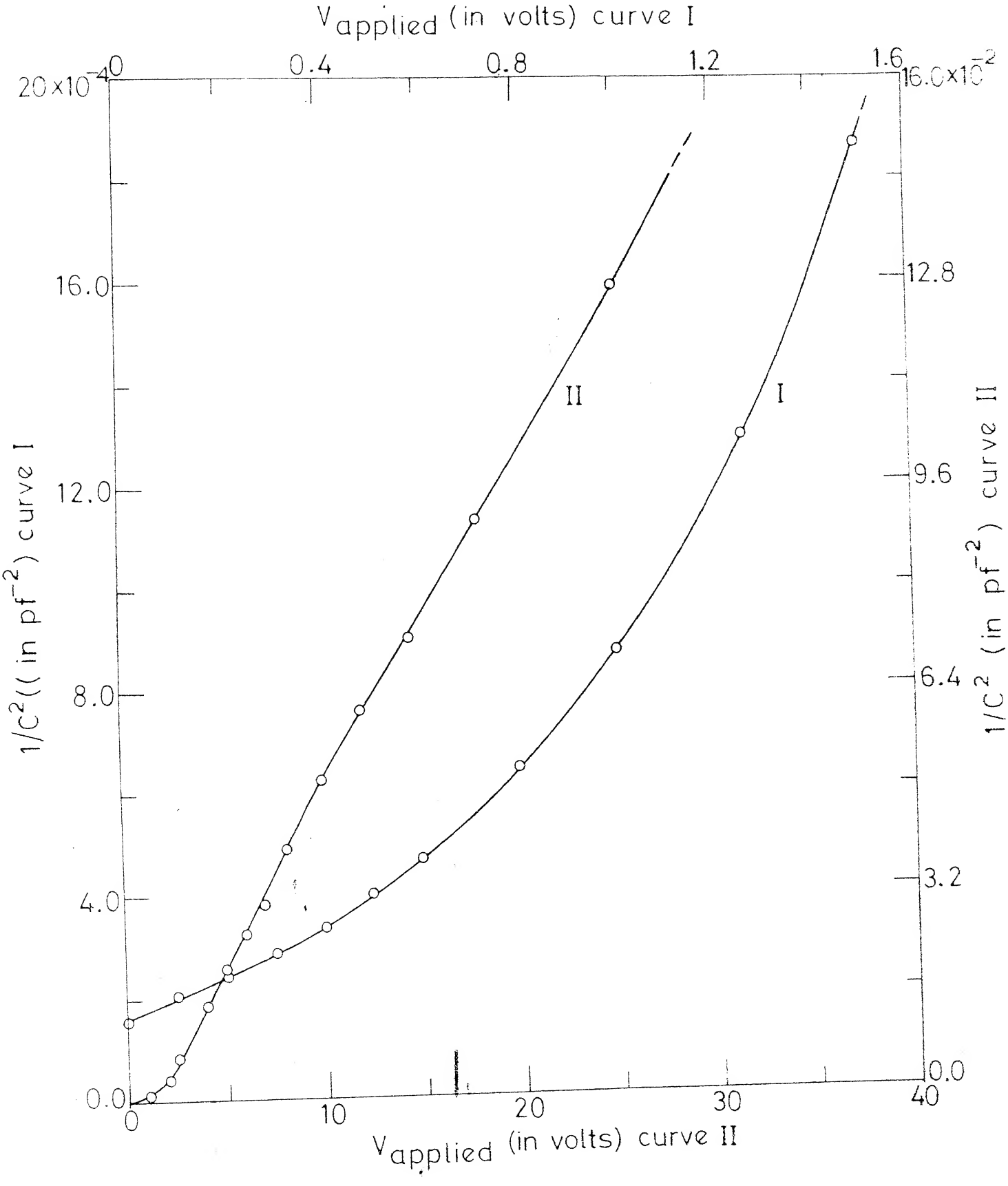
Vapplied (in volts) curve I
0
0.4
0.8
1.2
1.6
20x10⁻⁴
16.0x10⁻²
16.0
12.0
8.0
4.0
0.0
12.8
9.6
6.4
3.2
0.0
1/C²((in pf⁻²) curve I
1/C² (in pf⁻²) curve II
II
I
0
10
20
30
40
Vapplied (in volts) curve II

Fig. 23

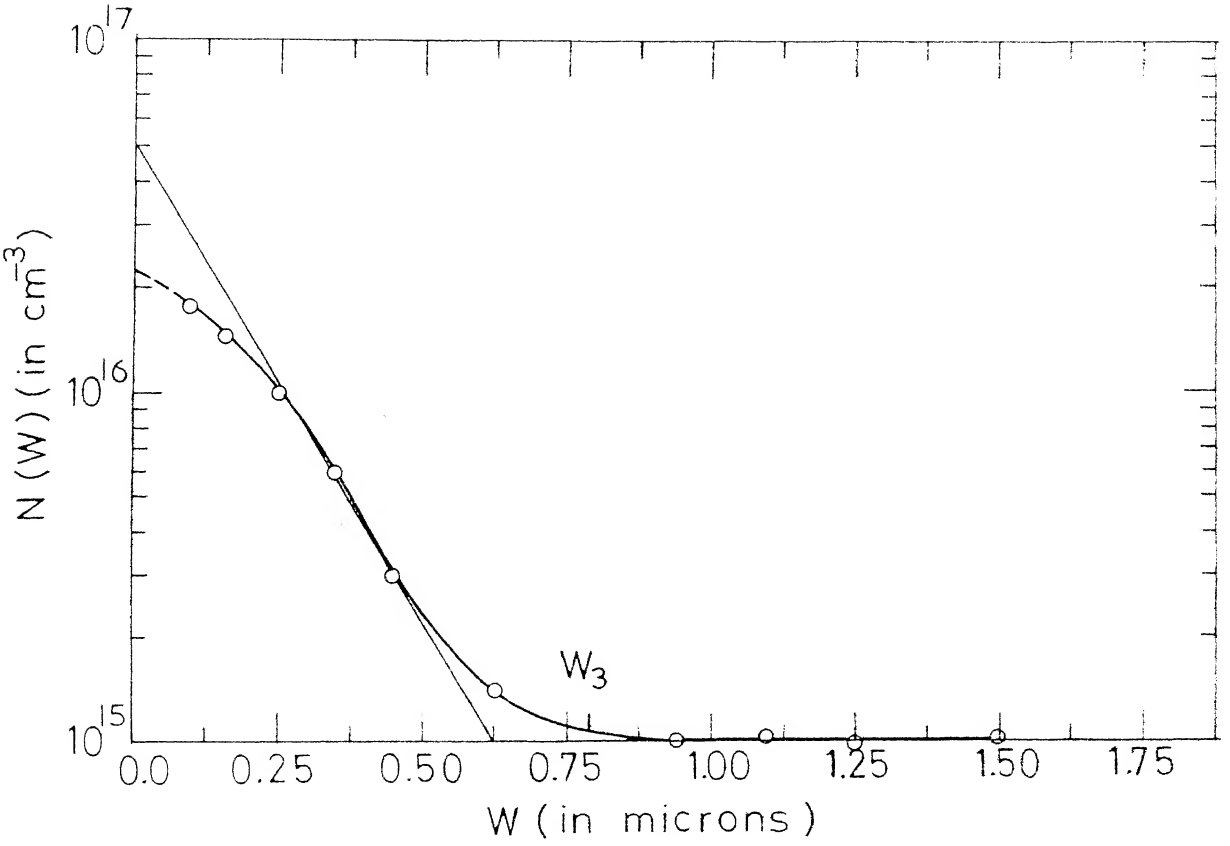
10^{17}
10^{16}
10^{15}
N (W) (in cm^{-3})
W_3
0.0
0.25
0.50
0.75
1.00
1.25
1.50
1.75
W (in microns)

Fig. 24

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